CPS SUPERSALT™ TECHNICAL USER'S MANUAL

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CPS SuperSALT™

Technical User's Manual

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INTRODUCTION

The Atari CPS SuperSALT™ Technical User's Manual is a reference guide for the service technician. The information presented in this manual, when used in conjunction with Atari training, enables you to use, and calibrate the CPS SuperSALT™ Diagnostic Cartridge (Super SALT) and the CPS SuperSALT™ Diagnostic Test Assembly (SuperSALT Test Assembly).

This Field Service Manual is organized in five sections:

- **THEORY OF OPERATION** - Overview of how SuperSALT and the SuperSALT Test Assembly work.
- **PROCEDURES FOR USING SUPERSALT AND THE SUPERSALT TEST ASSEMBLY** - Describes how to use SuperSALT and the SuperSALT Test Assembly to test a unit, the purpose of each test, the screens which display for each test, failing conditions and methods to remedy failures.
- **SUPERSALT TEST ASSEMBLY PCBA INSPECTION, CALIBRATION** - Procedure for inspecting, and calibrating the SuperSALT Test Assembly PCBA.
- **DRAWINGS** - Section to be used to hold the schematic for the SuperSALT Test Assembly.
- **SERVICE BULLETINS** - Section to be used to hold Field Change Orders, Upgrade Bulletins, and Tech Tips.

SECTION 1

THEORY OF OPERATION

OVERVIEW

The CPS SuperSALT Diagnostic Test Kit contains two major items: 1) the CPS SuperSALT Diagnostic Test Assembly (SuperSALT Test Assembly) which serves as an analog to digital converter and data switching unit; and, 2) the CPS SuperSALT Diagnostic Test cartridge (SuperSALT) which contains the software. This is the latest version of the Stand-Alone-Test hardware and software developed for testing and troubleshooting ATARI Home Computers.

SUPERSALT TEST ASSEMBLY

Figure 1-1 shows the SuperSALT Test Assembly which consists of the following series of functional blocks. These are discussed in the following paragraphs.

- o The precision power supply
- o The analog to digital converter (ADC)
- o The current to voltage converter
- o The Jack J1-J4 interfaces
- o The Serial Port Interface with associated serial test circuitry
- o The Error Display Port interface (Not Used; listed for clarity as J9)

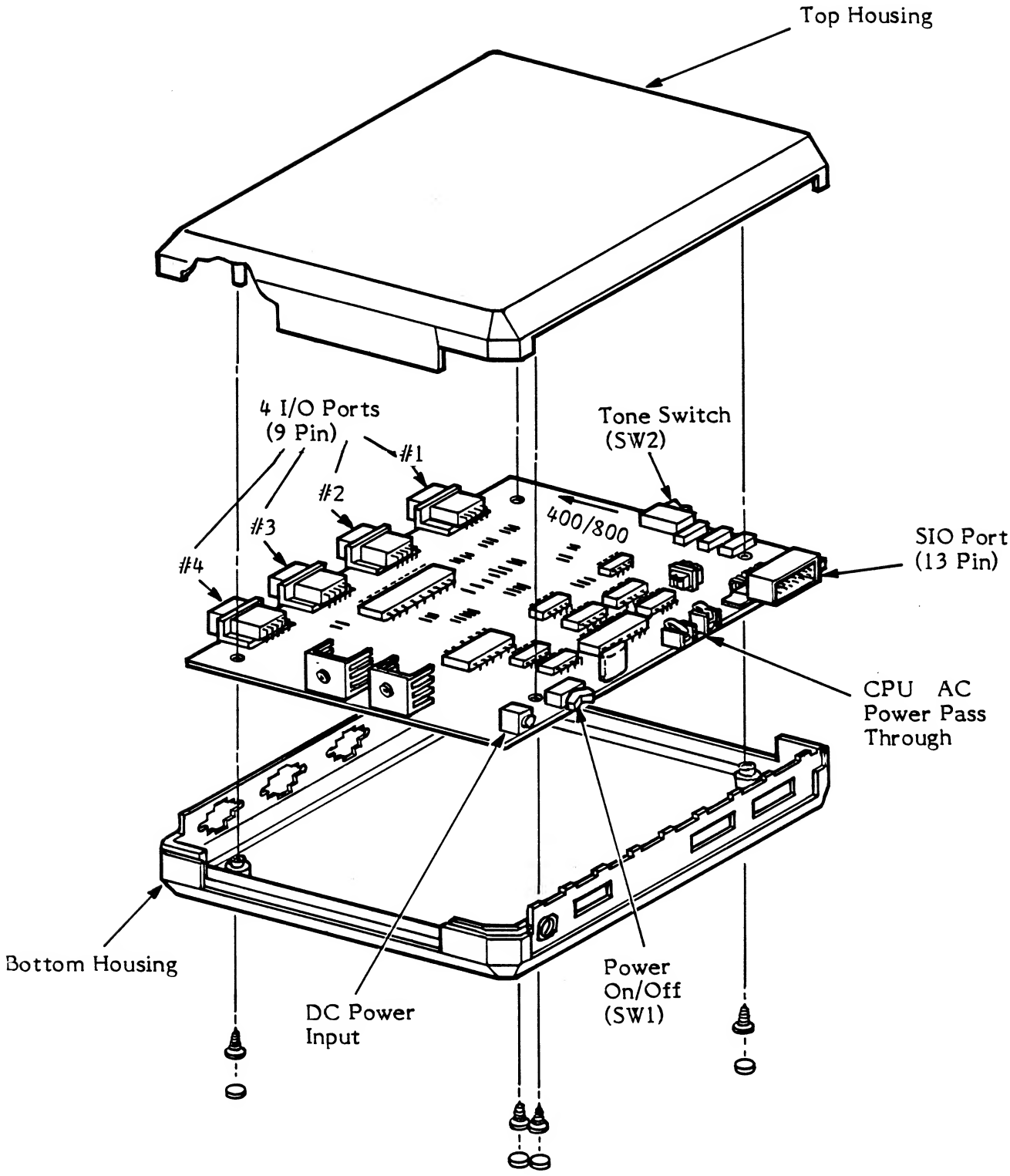


Figure 1-1. SuperSALT Test Assembly

THE PRECISION POWER SUPPLY

A precision power supply is used to provide an exact 6.00 volts as a reference for the analog to digital converter (ADC). SW1 enables the source of the voltage to be used to generate the precision reference.

The precision power supply is formed by one quarter of U10 (an OP AMP). This is used in a voltage follower configuration. Its input is fed from the center tap of a 100K 10-turn potentiometer in series with a 100K fixed resistor. This combination is in parallel with a 6.2 volt zener diode. The output of U10 is adjusted for exactly 6.00 volts. The adjustment must be exact since this is the reference for all voltages measured by the ADC.

In the 400 and 800 computers, a 12 volt source is measured to determine whether it is within specifications. This 12 volt source is scaled before feeding to the measurement circuitry to be within a range of 0-6 volts. Then the SuperSALT Test Assembly under software control, can adjust the voltage reading taken by the scale factor to present an accurate display of the voltage on the 12 volt line. This scaling is done by R39 and R40, which produces a voltage of exactly 5 volts for a 12 volt input.

THE ANALOG TO DIGITAL CONVERTER (ADC)

This is a 16 channel Analog to Digital Converter which uses the precision 6 volts as its reference. The converter is connected to measure and report the actual voltages present at various points. These voltage test points are as follows:

CHANNEL	CONNECTED TO
0	5 Volt Line Supplying the board
1	5 Volt Line from Serial Port of UUT
2	5 Volt Line from J1 port of UUT
3	5 Volt Line from J2 port of UUT
4	5 Volt Line from J3 port of UUT
5	5 Volt Line from J4 port of UUT
6	Ground Line from Serial Port of UUT
7	Ground Line from J1 port of UUT
8	Ground Line from J2 port of UUT
9	Ground Line from J3 port of UUT
10	Ground Line from J4 port of UUT
11	Motor Control Line from UUT
12	12 Volt line from Serial Port of UUT
13	Positive Half-Cycle Current drawn
14	Negative Half-Cycle Current drawn by UUT
15	Ground Line of power supply to Master interface board

UUT = UNIT UNDER TEST

All 5 volt inputs are pulled to ground with a 1K ohm resistor. All ground inputs are pulled to 5 volts with a 1K ohm resistor. This assures that a missing voltage or ground will definitely show up. (A floating input can cause a misleading input for the ADC).

All ADC sense lines (with exception of the Motor Control Line) that are connected to the Unit Under Test (UUT) are protected from static damage by clamping diodes to 5 volts and ground and by 10K ohm limiting resistors.

Channels 0 and 15 can be used as a self-diagnostic to determine the accuracy of the voltages used to power the SuperSALT Test Assembly. The other channels test that the UUT voltages are within specifications at the port connections (game ports 1-4; may include SIO, if applicable).

The UUT, with its cartridge program, selects which of the 16 channels are to be measured by placing the address within the low 4 bits of the output port (J1 or J3). Then it uses the SOD (serial output data) line as the control for the ALE (address latch enable) and the start conversion signal.

SOD is normally maintained high by the test program. The channel address is placed on the low 4 bits of an output port, then the SOD line is brought low. Lowering SOD latches the address into the ADC (analog to digital converter). Raising the line again starts the data conversion (Start line connected to ALE signal also) and clears any previous conversion results.

The ADC is a successive approximation type, whose conversion cycle is timed by one of the outputs of the baud rate generator circuitry. The conversion clock runs at 76.8KHz.

After completion of the ADC conversion, the OE (output enable) line may be brought high to feed the converted data onto the internal data bus where it may be read by the UUT through either J1, J2, or J3, J4 (port A or port B). This is done by lowering the Command line which is normally held high.

THE CURRENT TO VOLTAGE CONVERTER

The current to voltage conversion circuitry consists of a 0.1 ohm resistor and transformer T1. These sample the AC current and keep it isolated from the SuperSALT Test Assembly. The current samples are fed to two half-wave peak detectors to convert each AC half cycle to an equivalent voltage for the ADC to sense.

In operation, each half cycle of the AC voltage from the transformer is rectified by a 1N914 diode and presented to the input of a quarter of U10. The 10K ohm resistor to 5 volts in series with the 1N914 diode is used to establish an artificial ground for the AC waveform to prevent it from ever going below the Test Assembly ground. This prevents false readings from U10.

The OP AMP (U10) is used as a noninverting amplifier with the rectified AC waveform fed to the noninverting input. The rectified and filtered DC from the output is fed back through two 100K ohm resistors to the inverting input. The output of this section of U10 will be positive anytime the noninverting input is more positive than the inverting input and at ground otherwise.

The amount of DC voltage fed back is adjusted by the 100K ohm potentiometer to establish the gain of the circuit with a "known" load connected to the Test Assembly circuit. This establishes the calibration for the current measurement.

THE JACK J1-J4 INTERFACES

Jacks J1 through J4 correspond to player ports A through D of the UUT.

Testing The Voltage Supply Lines

Each player port has a 5 volt line and a ground line (pins 7 and 8 respectively). These are connected to the ADC channels as outlined earlier.

Testing The Data Lines

Each player port has 4 data lines (pins 1-4 inclusive), connected to port A or port B of the parallel port of the UUT.

In the UUT, the port lines are organized such that the lower 4 bits of port A connect to Player Port 1, the high 4 bits connect to Player Port 1. In port B, the low 4 bits are connected to Player Port 3, and the high 4 bits connect to Player Port 4.

This design takes advantage of the fact that port A or port B may each be assigned to be either an input or an output. The test software has been designed to assure that only one port will be assigned as an output at any one time. This allows the direct connection between Jack J1 pins 1-4 to Jack J3 pins 1-4, and J2 pins 1-4 to J4 pins 1-4. This is equivalent to a hardwired connection between the Input/Output (I/O) lines of Ports A and B of the parallel port.

By using this connection, with port A designated an input and port B as an output, the integrity of the ability of port A to input what port B outputs may be tested. Likewise by reversing the I/O assignments, the same data transfer integrity may be tested for the opposite direction.

Testing The Potentiometer Lines

Each of the player ports has two potentiometer input lines used for linear positioning type controllers (resistive input). Since there are 8 possible sources of input, there is a resistor (R1-R8), each connected to one of the potentiometer inputs. By setting only one of the bits of the I/O port high at a time, the correct operation of each of the pot inputs may be verified. The pot correspondence with which data bit is high is outlined in Table 1-1:

Table 1-1 lists data bit numbers. These correspond numerically to the I/O port data lines to which they are connected. In other words, data bits D0-D7 correspond to I/O port lines PA0-PA7 or PB0-PB7. In the 400/800 the SuperSALT Test Assembly ports A and B are hardwired together, so each bit D0-D7 represents the current state of either the corresponding port A or port B bit.

Table 1-1
DATA BIT NUMBERS

POT #	Which Data Bit Should Be High To Test It
0	D2
1	D3
2	D6
3	D7
4	D0
5	D1
6	D4
7	D5

Testing The Trigger Lines

Each player port is assigned one of the four trigger lines. To test each trigger line for the ability to show itself on or off, data lines are also used. The correspondence between data lines and trigger lines is shown in Table 1-2.

Table 1-2
DATA LINES/TRIGGER LINES

TRIGGER	Which Data Bit Low to Show Trigger is Pressed
0	D2
1	D6
2	D0
3	D4

THE SERIAL PORT INTERFACE

This interface connects to the serial I/O port of the UUT. It is designed to allow both synchronous and asynchronous testing of the serial port. A large portion of the remaining circuitry on the SuperSALT Test Assembly is dedicated to the serial communications.

Specifically:

U6, the baud rate generator
U5, the 8 bit data selector
U4, the binary counter
U3, the 16 bit data selector
U2, the mode control selector
U1, the mode control analog switch

Function Of The Baud Rate Generator (U6)

The baud rate generator, U6, is a programmable frequency divider. It takes a master clock frequency, in this case 1.8432 MHz, and provides as outputs frequencies appropriate to communications at various baud rates. The following outputs of the generator are used to provide the frequencies at which the Atari systems normally communicate:

OUTPUT #	Baud Rate
F1	9600
F3	4800
F5	2400
F7	1200
F8	600
F9	300

All of the above rates are selected by having input pin RSA at a zero voltage input. For those occasions when the baud rate generator is used for data transfer at 19200 baud, RSA is raised to a 1 by having the most significant data bit of the output port (A or B) at a zero level. The 19200 baud rate clock appears at output F5. This second mode is also used to provide the 76.8 KHz clock output from F1 when the baud rate generator is used as the clock input to the ADC.

Function Of The 8 Bit Data Selector (U5)

The 8 bit data selector controls which of the frequency outputs of the baud rate generator is to be applied to the serial port test circuitry. Bits D4, D5, and D6 (LSB to MSB) of the output port control which of the frequencies to apply for the test.

Function Of The Binary Counter (U4)

The binary counter is provided to allow a hardware generated data-byte to be transmitted to the UUT. This counter provides the data input to U3, to select which of 16 data bits is to be "transmitted" to the UUT.

Function Of The 16 Bit Data Selector (U3)

This data selector forms a hardwired hexadecimal 55 which can be transmitted to the UUT. The outputs from U4 are used to select one of 16 possible inputs to apply to a single output. For serial communications, this hardwired 55 consists of bits defining one start bit, 8 data bits, and 7 stop bits.

Function Of The Mode Control Selector (U2)

This integrated circuit combines the signals MC (motor control) and D2 (data bit 2 from the I/O port) to select whether there should be any clock or no clock frequency applied to the clock input (pin 2) of the UUT serial bus. Controls the C input of U1.

The type of clock which will be applied here is selected by the state of the A input of U1.

Function Of The Mode Control Analog Switch (U1)

There are three separately controllable analog switches in this circuit. All are fully bidirectional and fully isolated from each other. The functions of each section are described below:

Section A - Common terminal, used as output, connected to UUT pin 1 and to Section C, input X. Input is called the Bidirectional Clock.

Input X - Selects external baud rate generator or external audio test.

Input Y - UUT clock out.

Section B - Common terminal, used as output to terminal 3 of UUT serial bus. Known as Serial Input to UUT.

Input X - hardwired 55 to be sent to UUT (see description in previous section).

Input Y - Loop back UUT data in from UUT data out.

Section C - Common terminal, output to UUT pin 11 (Audio Input).

Input X - selects the output from channel A.

Input Y - no connection (unit becomes "quiet" when this mode selected).

MOTOR CONTROL LINE MODIFICATIONS

The motor control line requires some noise filtering. This necessitates the addition of a capacitor from MC to ground. To allow the capacitor time to charge adequately, it is necessary that the software allow a 10 millisecond interval from the time the MC changes state until the voltage on it is to be read by the ADC.

To provide the extra drive current required to support the added capacitor, the Motor Control line is now buffered under all conditions except when it is being measured to determine its output voltage.

SECTION 2

PROCEDURES FOR USING SUPERSALT AND THE SUPERSALT TEST ASSEMBLY

This section describes how to use CPS SuperSALT and the SuperSALT Test Assembly to test a unit, the purpose of each test, the screens which display for each test, failing conditions and methods to remedy failures.

SUPERSALT FEATURES

Overview

The CPS SuperSALT Diagnostic Test Kit (FK100331) contains two major items: 1) The CPS SuperSALT Diagnostic Test Assembly (SuperSALT Test Assembly), Part No. FA100332, which serves as an analog to digital converter and data switching unit; and, 2) The CPS SuperSALT Diagnostic Cartridge (SuperSALT), Part No. FD100335, which contains the software.

The SuperSALT Test Assembly tests voltage, SIO and the controller ports. It loops digital data from one controller port to another and checks the results, or converts analog signals and levels to digital data and returns the data for analysis via the SIO port to the unit under test.

The software contained in SuperSALT is designed to test all areas of the system: MPU, RAM, ROM, SIO port, Controller ports, ANTIC, GTIA, POKEY and Keyboard, as well as Video and Audio Logic.

Five functional divisions in the software menu include:

- o PERFORMANCE TEST
- o INDIVIDUAL TEST
- o EXTENDED UNIT TESTS
- o CHANGE TEST OPTS
- o SHOW ERR SUMMARY

Each of these functions contains another menu to further control and/or tailor test selections. A brief discussion of each test follows.

PERFORMANCE TEST

Performance Testing is the sequential execution of predetermined test routines that cannot be changed. Once started, all tests execute unless BREAK or RESET is depressed. This action halts testing.

EXTENDED UNIT TEST

Extended Unit Testing is much like Performance Testing in that it is a sequence of tests. The difference is that the sequence to be executed may be added to or deleted from and the order rearranged. Thus, the technician may tailor the testing to specific problems.

INDIVIDUAL TEST

Individual Testing allows a specific program to be executed in order to test a suspect function.

CHANGE TEST OPTS

The Change Test Opts feature allows you to change testing parameters for further tailoring of any of the test procedures. You may select any of the following features in any combination:

- Continuous or single pass testing (all tests).
- Testing Sequence (when applicable) sequential or random.
- Display time, two to twenty seconds in two second intervals. You can also select an infinite display duration called "RTN", which loops through a test or tests until you press RETURN.
- Test Group, selection control of the programs which run under the Extended Unit Testing option.

SHOW ERR SUMMARY

The Show Err Summary screen displays a tabulation of errors detected in each test executed.

NOTE:

1. All counters in Error Summary are reset if SYSTEM RESET is pressed.

2. For the Executive Menu, OPTION displays the selected menu. SELECT moves the pointer (title turns black) to a new selection and BREAK returns to previous menu.

3. BREAK returns to previous menu during any testing. Be patient. Some test must complete before the software recognizes the BREAK key. INDIVIDUAL TESTS, CHANGE TEST OPTIONS and SHOW ERR SUMMARY menus have special instructions (different from other test menus) for execution. NOTE these instructions for proper execution, at the bottom of the display screen.

SUPERSALT TESTING PROCEDURES

Equipment Required:

- a 9V Power Adaptor
- a television, properly adjusted
- an Atari CPU to be tested

- o CPS SuperSALT Diagnostic Test Kit (FK100331) which consists of the following items:
  CPS SuperSALT Diagnostic Test Assy (FA100332) (See Fig. 1-1)
  CPS SuperSALT Diagnostic Cartridge (FD100335)
  Cable Assy, AC Jumper (FA100336)
  Cable Assy, Dual 9-Pin, 30" (FA100765)
  Cable Assy, Serial I/O (CA014122)
  CPS SuperSALT Technical User's Manual (FD100770)

Procedure:

Perform the following functions exactly as described below to connect the Super SALT Test Assembly (FD100332).

1. Connect the I/O Ports (9-Pin) between the computer and the SuperSalt Test Assembly as directed below:

   A. 400/800 (Front Port CPU's)
      1) Computer Controller Port 1 to SuperSALT Test Assembly Port 4
      2) Computer Controller Port 2 to SuperSALT Test Assembly Port 3
      3) Computer Controller Port 3 to SuperSALT Test Assembly Port 2
      4) Computer Controller Port 4 to SuperSALT Test Assembly Port 1
   B. XL Series (ALL)
      1) Computer controller Port 1 to SuperSALT Test Assembly Port 4
      2) Computer controller Port 2 to SuperSALT Test Assembly Port 3.

2. Connect the SIO Port (13-Pin) on SuperSALT Test Assembly to Computer Peripheral Port.

3. CPU AC Power Pass Through:

   A. 400/800/1200XL
      1) Insert the male connector from the Computer's power adaptor module into either one of the two female connectors.
      2) Insert either of the male connectors of the Power Jumper Cable into the other female connector.
      3) Insert the other male connector of the Power Jumper Cable into the Computer's power input.
   B. XL Series Computers*
   Connect the computer's Power Supply per instructions found in the Owner's Manual.
      4) Connect the SuperSALT Test Assembly Power Adaptor to the SuperSALT Test Assembly.
   NOTE: The XL* Series Computers and the SuperSALT Test Assembly must be powered by their respective power supply.
      5) Set the Tone Switch per the following instructions:
         A. 400/800
         Toward controller ports
         B. XL Series
         Away from controller ports

   * = 600XL, 800XL and 1450XL

Connect the television. Insert the SuperSALT cartridge and turn on the power. The screen displays the Title Screen (See Figure 2-1).

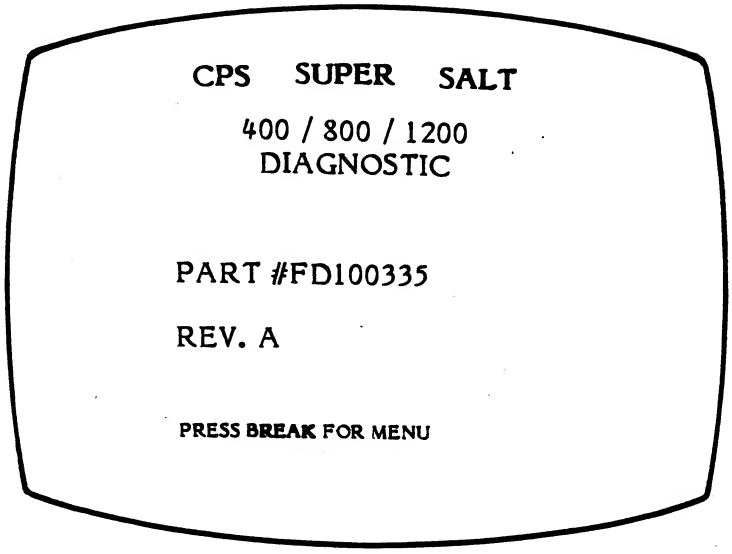


Figure 2-1. Title Screen

Depress the BREAK key to continue. The screen displays the SuperSALT Executive Menu (See Figure 2-2).

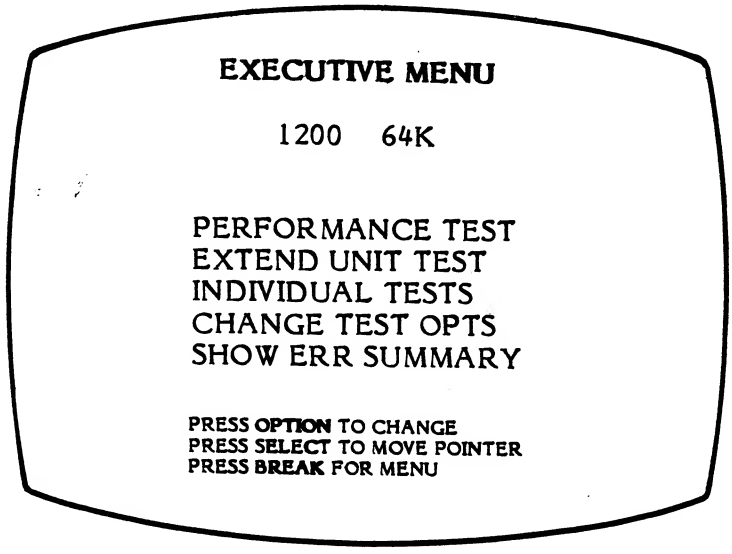


Figure 2-2. Executive Menu Screen

PERFORMANCE TEST

The Performance Test is automatically highlighted when SuperSALT initializes. This must be the first test run. The Performance Test does require the SuperSALT Test Assembly.

Press the Option key to show the main menu. Verify that the SuperSALT Test Assembly is connected, I/O cable is installed correctly and power is on.

Press START. The Performance Test Screen is displayed (See Figure 2-3).

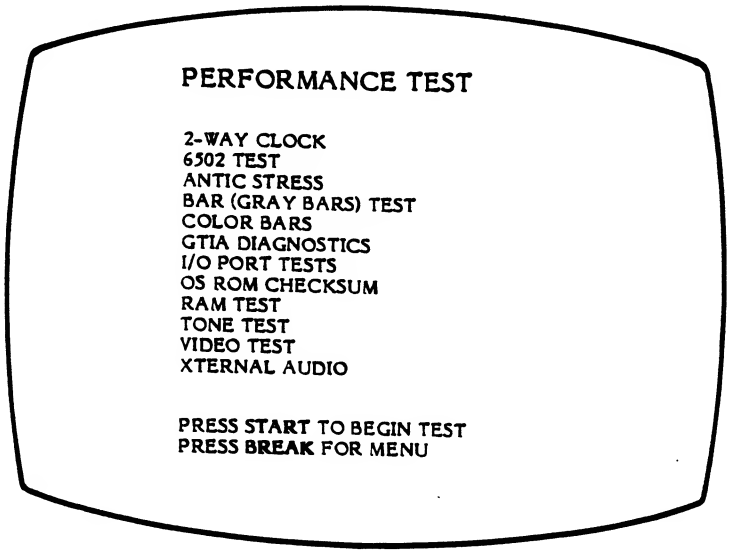


Figure 2-3. Performance Test Screen

2-WAY CLOCK TEST

As shown on the screen (See Figure 2-4), if tones are heard the test passes. If tones are not heard, verify the following.

Verify: TV volume is up
SuperSALT Test Assembly is properly connected
SuperSALT Test Assembly is powered up
SuperSALT Test Assembly Tone Switch is set correctly

Execute the Performance Test again. If failure persists go to the Individual Test Menu to loop on test for scoping. If all signals are found, replace Pokey I.C. - U20.

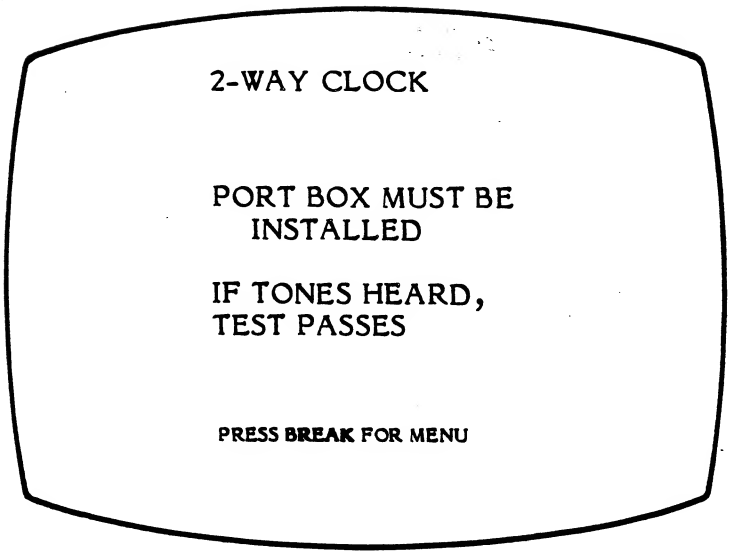


Figure 2-4. 2-Way Clock Screen

6502 TEST

The 6502 Test screen (See Figure 2-5) is the next test performed. A single pass executes 100 cycles before displaying this screen. One cycle is a complete execution of all 151 operation codes performed by the 6502 CPU.

One of four conditions will exist as a result of 6502 Test execution. They are:

1. The test passes, and the screen display shows the number of complete cycles; or,

2. The test fails due to an error detected in the low bank of RAM, reporting a RAM error (verify with RAM Test); or,

3. The test fails due to an incorrect result detected during the attempted execution of a CPU instruction, shown on SHOW ERR SUMMARY; or,

4. The test never completes due to a faulty CPU (or other associated component) causing the CPU to execute an illegal instruction, and potentially ending up in an undefined execution mode (usually a "lock-up").

Failures of type 2 should be verified by the RAM Test. If RAM Test does not fail, replace 6502 IC - U10.

For failures of types 3 or 4 - replace 6502 IC - U10.

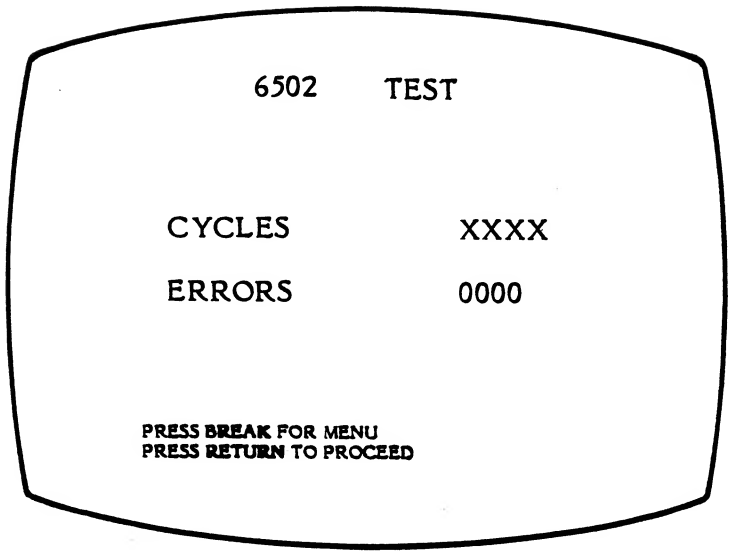


Figure 2-5. 6502 Test Screen

ANTIC STRESS TEST

The purpose of the ANTIC Stress Test (See Figure 2-6) is to assure that all possible display modes of the ANTIC are functioning. This test is operator interactive. The only way to determine whether the unit is functioning correctly is to judge the correctness of the display. If its physical appearance does not match that shown, there may be a problem with one or more display modes of the ANTIC.

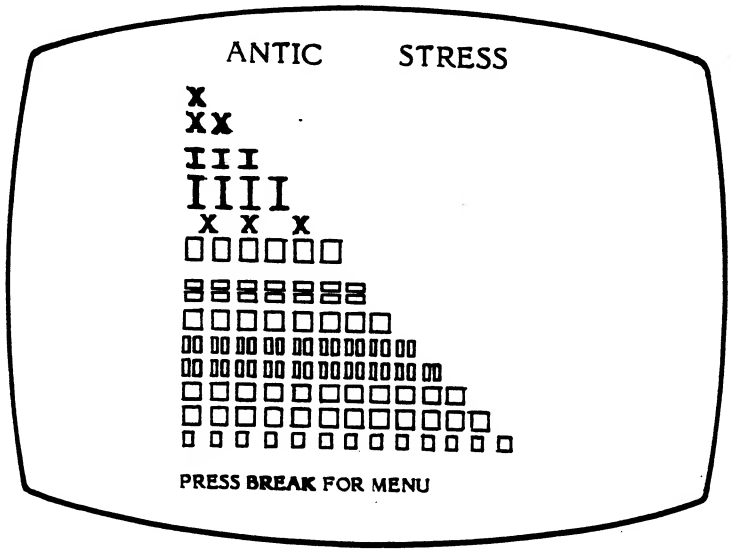


Figure 2-6. ANTIC Stress Screen

The top of the screen has the title, ANTIC Stress, first in capital letters and switches to lower case. The top X appears as an X then as an inverse X. The fourth row of characters, four Capital I's, scroll upward and disappear. Then they scroll downward back onto the display. The fifth row of characters, three X's, scroll to the right. As they scroll a fourth X appears from the left until it is a full character. The row then scrolls to the left until only three X's are on the screen again. All other rows of blocks must have the shape indicated, must be properly, spaced and separated. The bottom of the screen has the instructional message with the word BREAK flashing on and off. All items mentioned must be present and correctly displayed. Color is not important, only function. Any failure above indicates a faulty ANTIC.

BAR TEST

This test verifies that the GTIA is generating four LUM bits (LUM0-3).

Figure 2-7 is a display of the Gray Bar Test. The screen is divided into eight equal sized horizontal bars. The bar at the top of the screen should be black and subsequent bars should progress to white at bar eight. The bars should lighten in even shades. The screen should be steady and unchanging. These lines may have minor glitches at their edges. A thin white line should always appear just over the top (black) bar. No color should appear anywhere on the screen. The areas above the top (black) bar and below the bottom (white) bar are of no importance to this test. This test should be left on for at least 10 seconds to ensure that there is no "flashing" of color or shifting of the gray bars.

Missing bars, bars of the same exact shade, colored bars or more than eight bars indicate a faulty GTIA.

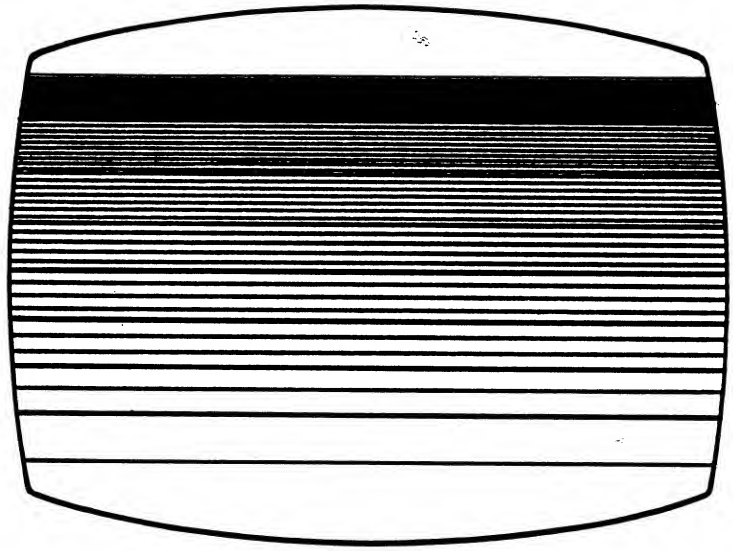


Figure 2-7. Bar Test Screen

COLOR BARS

This test verifies and allows for adjustment of the color circuitry. Figure 2-8 is a black and white representation of how your television display screen should appear.

A 15-color rainbow scale is displayed above the reference bar with a single color bar below. The color bars directly above and below the reference bar should be the same color (goldenrod). If not, proper adjustment of a variable resistor makes the color bars above and below the gray reference bar identical thus adjusting the color frequency of the console to the proper setting.

The operator should verify proper operation of the unit by making this adjustment with the unit displaying consistent color within the entire span of each bar on the screen. Minor glitches on the edges of the color bars are acceptable.

Any missing bars or lack of color indicate failures. Failures in order of importance are:

1. Color adjustment - Adjust R43
2. Faulty GTIA
3. Faulty ANTIC
4. Bad or incorrect crystal - Y1 (NTSC 3.579545 MHz, PAL 3.546894 MHz)

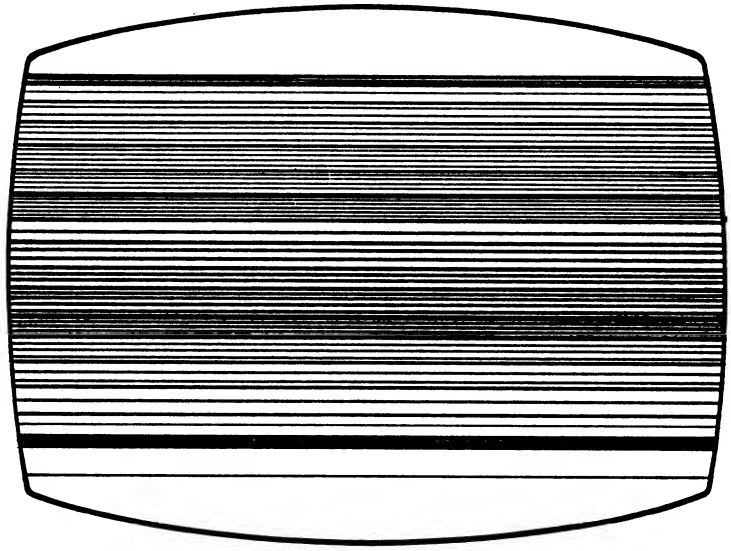


Figure 2-8. Color Bar Screen

GTIA DIAGNOSTICS

NOTE: The following description is lengthy. It is suggested that the technician first watch the GTIA Diagnostic function several times using Individual Test Mode. Then read this analysis procedure.

The three GTIA Diagnostic Screens (See Figures 2-9 thru 2-11) which follow are black and white representations of your television display.

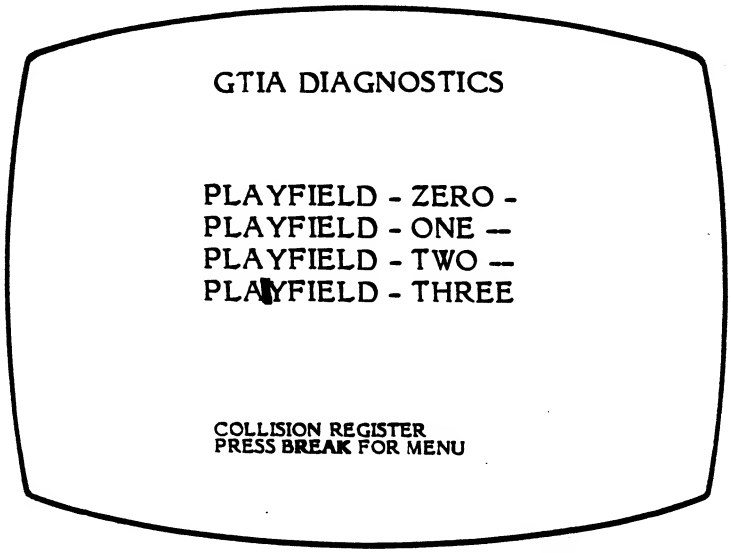


Figure 2-9. GTIA Diagnostic Screen (Part 1)

Part 1

There are four horizontal bars formed on the screen by the words PLAYFIELD ZERO, ONE, TWO, and THREE (Refer to Figure 2-9).
Moving in between the horizontal bars, evenly distributed across the screen, are two sets of rectangles. The first rectangle is formed by players 1 through 4. The second rectangle is formed by missiles 1 through 4.

All of the player-formed figures should be the same size. The missile-formed figures will vary in size on the screen.

This character formation verifies the capability of the GTIA to control the size of the players and missiles correctly. The players are not actually the same size, even though they appear as though they are. This also verifies capability of the GTIA to move missiles and players through the playfields, and detect collisions between players and missiles.

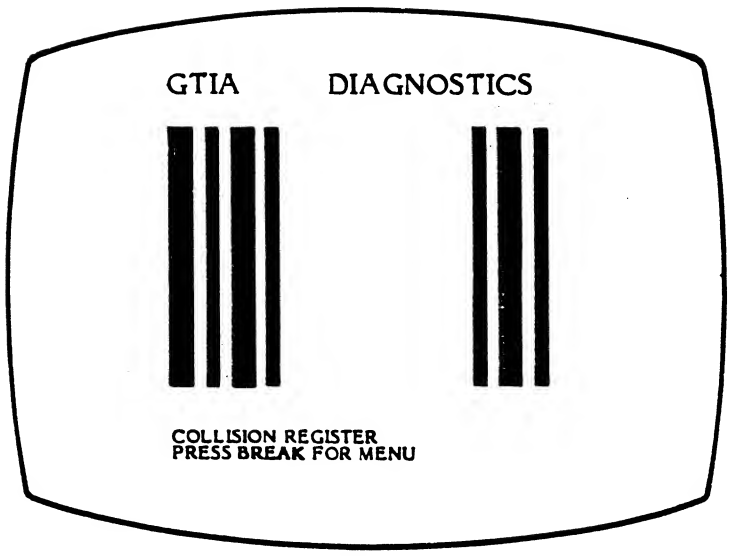


Figure 2-10. GTIA Diagnostic Screen (Part 2)

Part 2

There are two sets of four vertical bars (Refer to Figure 2-10). The narrow bars are missiles, the wide bars are players. Both types of bars are rotated through their respective sets. This tests the capability of GTIA to detect collisions on a non-playfield type of operation with multiple players.

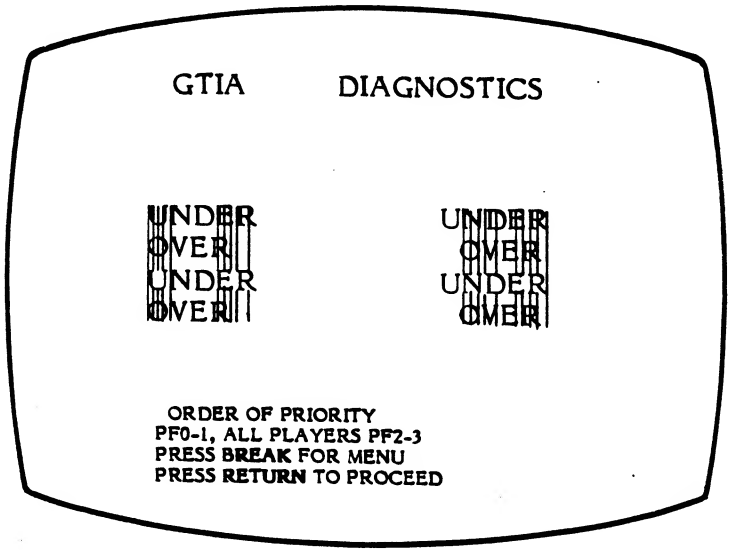


Figure 2-11. GTIA Diagnostic Screen (Part 3)

Part 3

There are two sets of words, UNDER, OVER, UNDER, OVER (from top to bottom) (Refer to Figure 2-11). These sets of words are striped with thin black bars running vertically top to bottom. The bars should be under the word UNDER and over the word OVER as indicated. Note the text window at bottom of the screen identifies the particular player, missile, playerfield combinations in use.

Any failure indicates a faulty GTIA. All test must function properly.

I/O PORT TESTS

NOTE: Must have the Test Assembly connected and operational.

Figure 2-12 and 2-13 are black and white representations of your television displays.

The following tests are performed:

a. Voltage levels on each of the ports +5V, ground.

b. Ability of any and all of the I/O ports to act as an input or as an output.

c. Exercises the trigger lines in each port.

d. Exercises the pot lines in each port.

e. Tests the motor control line, the command line, the interrupt line of the serial port and serial input and output data lines.

f. Verifies the capability of the unit to communicate in ASYNC mode with peripherals at baud rates of 300, 600, 1200, 2400, 4800, 9600, 19200 and synchronous at 19200.

Three tests are performed. They are:

- o Asynchronous communications
  1) Six Baud rates are used: 300, 600, 1200, 2400, 4800 and 9600.
  2) The Test Assembly transmits an ATASCII "55" to the UUT. If data is mismatched or a frame error occurs, up to 15 retries are allowed requiring 0.8 seconds (time enough for the Test Assembly to transmit 15 characters at 300 baud). If no data is received unit is failed as a timeout.

- o Synchronous Communication
  1) Uses UUT clock.
  2) Fifteen Bytes are transmitted at 19.2K baud. One correct byte of the fifteen is a pass.
  3) If some fatal mode is encountered, the async tests are begun again to "flush out" the system. This is tried three times before the unit is failed.

- o Synchronous Communication
  1) Fifteen Bytes are transmitted at 19.2K baud synchronously using the external clock on the Test Assembly. One byte out of fifteen is a pass.
  2) If some fatal mode is encountered, the async tests are begun again. This is tried three times before failing the unit.

Baud Rate Failure Decode

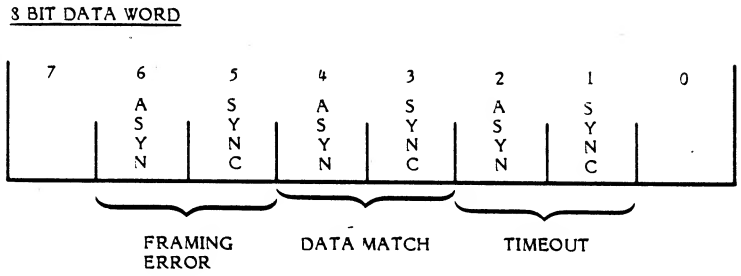
To gain a complete understanding, perform the following example.

1) Press System Reset
2) Go to Individual menu
3) Unplug Data I/O cable from the Test Assembly
4) Select I/O testing by pressing "I"
5) When testing is complete, go to Error Summary, Baud Rate failures (Fig. 2-35).

This shows one cycle and two errors.
NOTE:Baud Rate failures are in two categories (See the figures below).

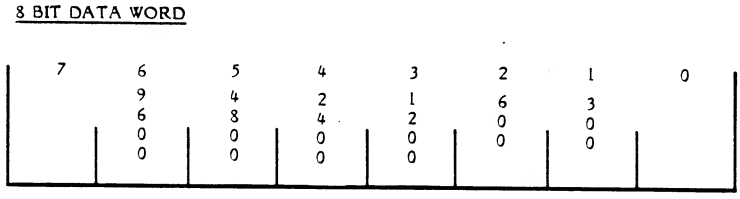
Error Type simply defines type of failure and how many.

Error Code decodes as follows:



Note the 6 in the sync baud counter. The six (6) decodes in the figure above as a Synchronous & Asynchronous Timeout failure.

Since any synchronous failure causes all asynchronous test to be run, the next three lines determine which baud rates failed. They decode as follows:



Thus, asynchronous failed timeout at all baud rates, as the "7E" code indicates.

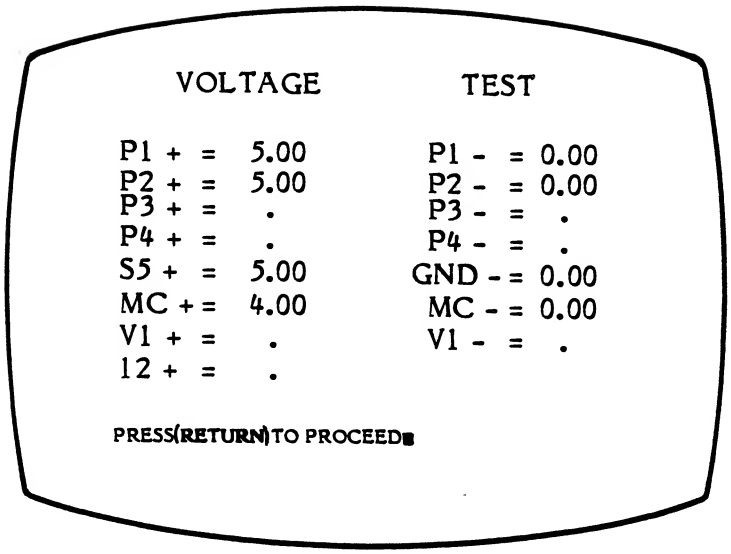


Figure 2-12. I/O Port Tests Screen (Voltage Test)

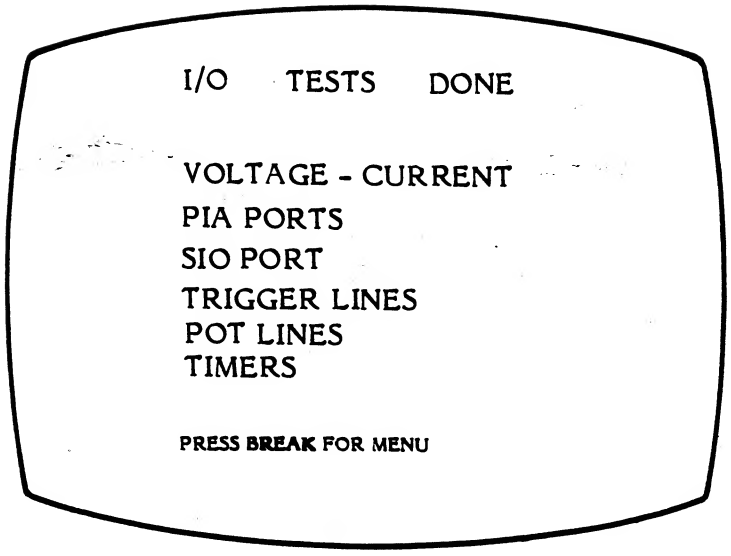


Figure 2-13. I/O Port Tests Screen (I/O Tests Done)

The screen is cleared. Voltage Test (Refer to Figure 2-12) is displayed along with the voltages found as appropriate to the unit. **NOTE:** No current measurements are available at this time. The screen again is cleared and displays in the center, the following list of tests (Refer to Figure 2-13):

VOLTAGE & CURRENT
PIA PORT
SIO PORT
TRIGGER LINES
POT LINES
TIMERS

The test names are white (indicates test is in progress) and changed to green at test completion, REGARDLESS of pass or fail conditions. Reference the SHOW ERR SUMMARY Screen, Schematics and Silkscreens for particulars and troubleshooting. NOTE: During Voltage/Current testing (Refer to Figure 2-12), green values indicate a pass condition and red indicates a failure. Troubleshoot accordingly.

NOTE: I/O Voltage Error Display is shown only on I/O Port Tests Screen (Voltage Test). It is recommended that you go to Individual Test and run the I/O test again. See Table 2-1 for voltage limits.

IMPORTANT: All other failures usually indicate a bad PIA or POKEY IC.

ALWAYS verify the Test Assembly hook-up, setting of switches and power on, for any I/O failures. Execute this test again. Excessive failures; i.e., all voltages are incorrect, may indicate Test Assembly failure or lack of power.

Table 2-1
Voltage High (VH) and
Voltage Low (VL) Limits

I/O Test uses Voltage High (VH) and Voltage Low (VL) limits as follows:

	VH	VL
P1-4 +	+5.24V	+4.72V
P1-4 -	+0.748V	+0.00V
S5 +	+5.24V	+4.72V
GND	+0.21V	+0.00V
MC +	+5.24V	+2.85V
MC -	+0.748V	+0.00V
VI +	4.048V	+0.936V
VI -	4.048V	+0.936V

OS ROM CHECKSUM

Figure 2-14 shows the OS ROM Checksum test.

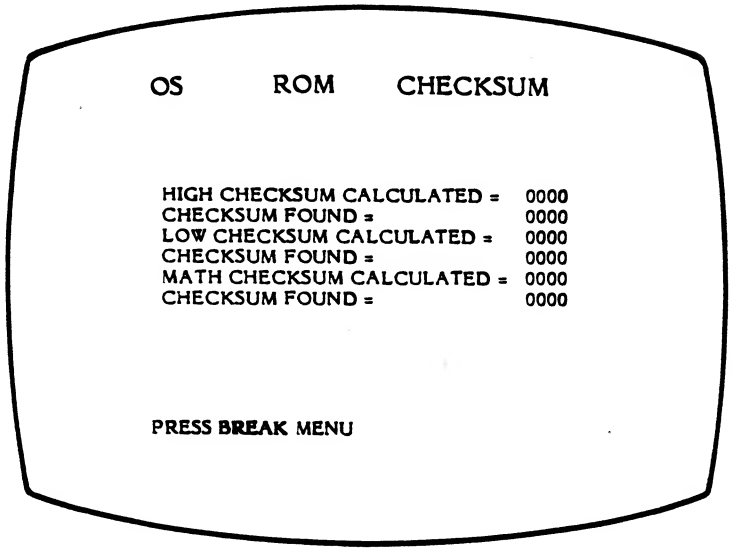


Figure 2-14. OS ROM Checksum Screen

This test reads the OS ROM and performs a checksum calculation. The test then retrieves the stored checksum word from the ROM and compares it to the calculated value. Value differences indicate a failure of the ROM or support circuits.

RAM TEST

Figures 2-15 and 2-16 show the RAM Test screens.

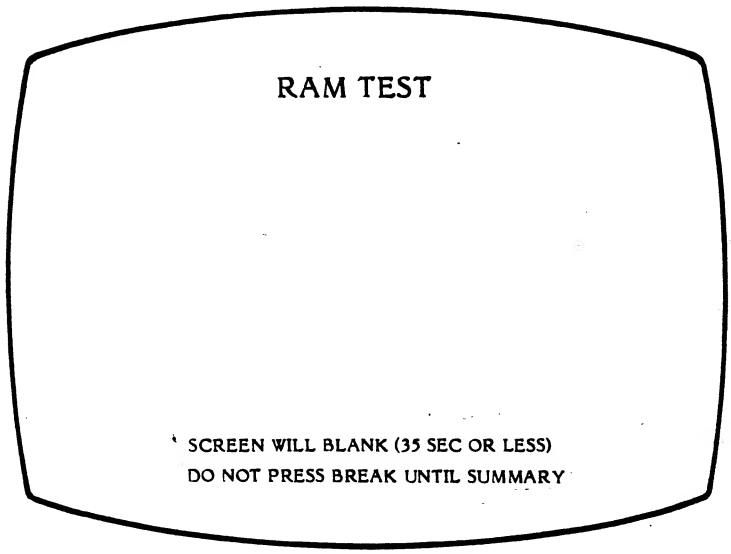


Figure 2-15. RAM Test Screen (Screen 1)

** Break message only appears on 64K systems

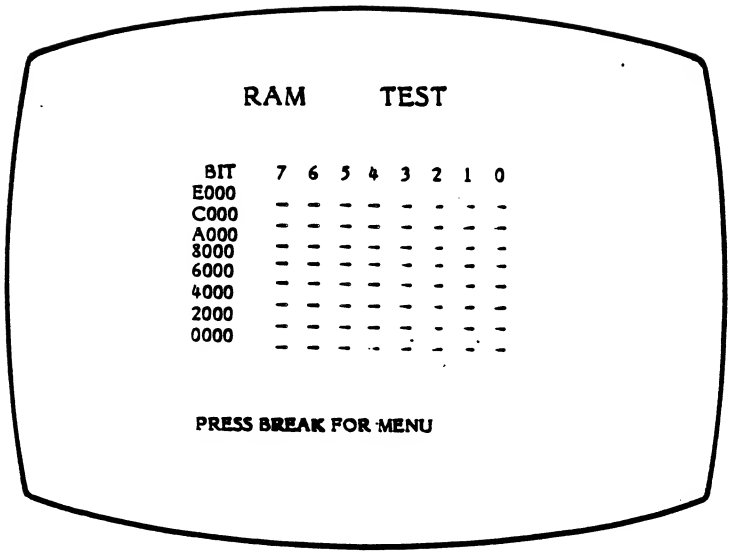


Figure 2-16. RAM Test Screen (Screen 2)

The following types of tests are performed on the UUT.

a) Marching 1's thru memory to test internal chip decode
b) Marching 0's thru memory to test internal chip decode
c) Fill memory with variable data field
d) Fill memory with compliment of above
e) Test for fail with constant data
f) Test for fail with random data
g) Wait on refresh fail to insure proper refresh timing during blank screen

Each 8K block of memory takes 5.5 sec to test. For example, 48K as in the XL series computer takes 33 seconds (5.5 X 6 = 33) which is approximately how long the screen is blank.

Note the text window in Figure 2-15. The screen goes blank for 35 seconds or less while REFRESH testing is performed. The screen then returns with the error summary. Refer to Figure 2-16 for data bit failures. Data bit failures are indicated by inverse video F.

On any RAM failure refer to HCD Tech Tip #20 and verify that the correct ANTIC revision has been installed. If the proper revision is installed, replace the appropriate RAM IC and retest. If unit still fails, then replace the ANTIC or appropriate support logic.

TONE TEST

Figure 2-17 shows the Tone Test screen.

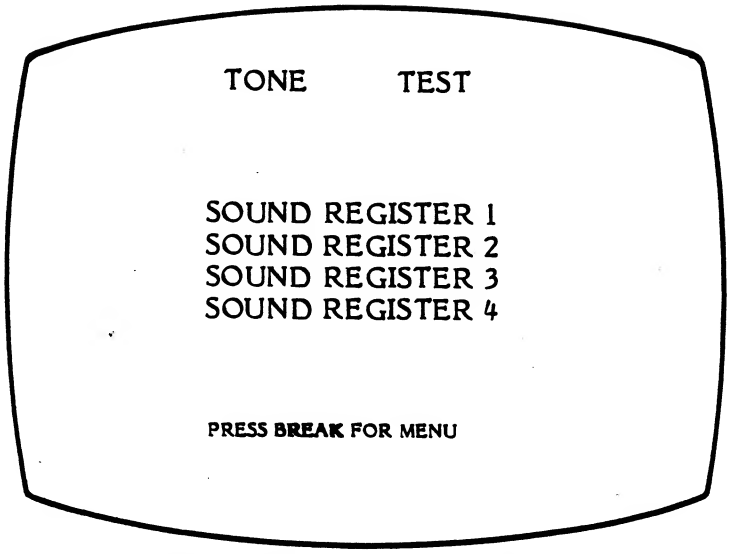


Figure 2-17. Tone Test Screen

The words Sound Register 1,2,3 or 4 are highlighted as each register is tested. The test consists of a sweep of each register from the highest tone to the lowest. Failures are indicated by missing tones. Failures indicate a faulty Pokey I.C., failure of the audio support circuit (U8) or 4.5MHz oscillator misalignment or failure. Adjust 4.5MHz or troubleshoot and repair.

VIDEO TEST

This test verifies the console's ability to generate a video (TV) display. This test also checks for pattern sensitivity of the ANTIC chip.

The screen shown (See Figure 2-18) is the display for Video Test. **NOTE:** This is a black and white representation of a colored screen.

The screen should have a black background with eight vertical bars. Half of the vertical bars should be narrow, and the other half, much wider. A horizontal bar should appear across the top of the screen. From the left to right, the shade of color on the horizontal bar should change. On the right of the bar, two Vs should be displayed, right side up; one in normal video and the other in inverse video.

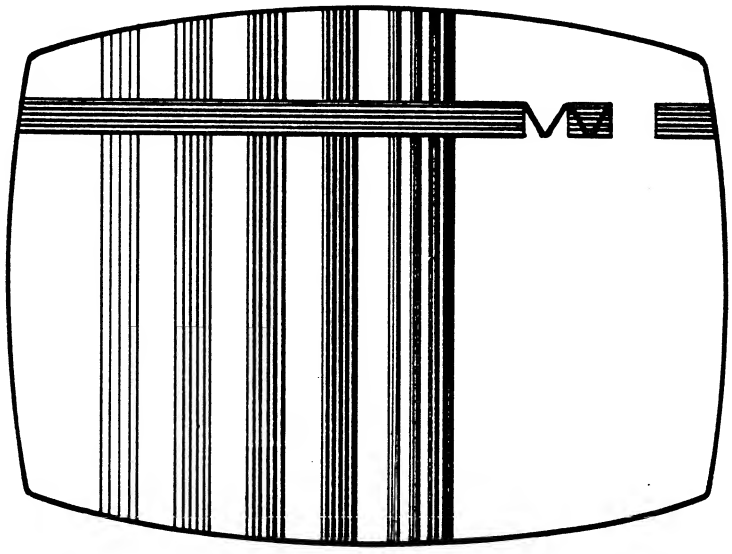


Figure 2-18. Video Test Screen

XTERNAL AUDIO

NOTE: This test requires the SuperSALT Test Assembly.

Figure 2-19 shows the Xternal Audio Menu.

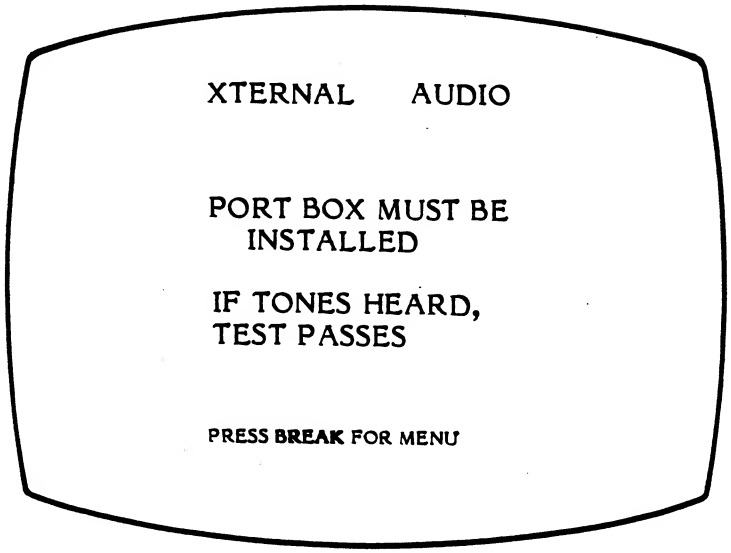


Figure 2-19. Xternal Audio Screen

This test uses the SuperSALT Test Assembly to simulate external audio as produced by the cassette recorder or other external audio device. If tones (a short melody) are heard, the test passes. If not, failure is probably the POKEY IC. Other possible failures are as follows:

1) TV Volume
2) 4.5MHz Oscillator adjustment
3) Sound mixer, IC U8 and support circuitry

The PERFORMANCE TEST menu is returned to the screen. This ends the PERFORMANCE TEST. If all tests pass, the unit is satisfactory. If the unit fails any of the tests,* use the INDIVIDUAL TESTS along with the CHANGE TEST OPTS to troubleshoot the faulty circuit.

*Press BREAK to access EXECUTIVE MENU screen.

INDIVIDUAL TESTS

NOTE: Only the tests not previously discussed are shown. Reference PERFORMANCE TEST for tests not shown here.

Individual tests discussed earlier allows the technician to execute a particular test indefinitely and for most tests to control the display time. The details of control are shown in EXTEND UNIT TEST. Press SELECT to move pointer to INDIVIDUAL TESTS. Press OPTION to display menu (See Figure 2-20). Note instructions at bottom of menu.

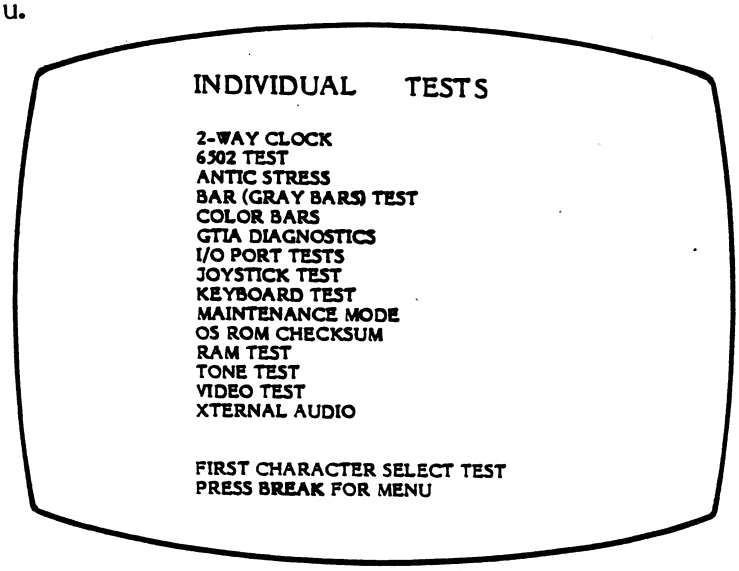


Figure 2-20. Individual Tests Menu Screen

JOYSTICK TEST

Figure 2-21 shows the Joystick Test Screen.

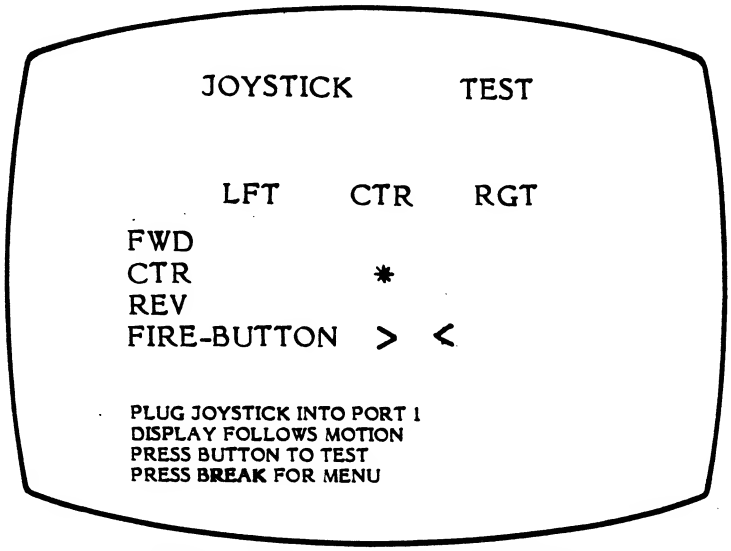


Figure 2-21. Joystick Test Screen

This test is used to verify correct Joystick and Trigger operation. It is assumed that I/O Port Testing is complete and passed. In other words, a working unit.

Insert the Joystick plug into Port 1 on the console. The * (asterisk) displayed on the screen should remain centered. The * should follow the Joystick action as you move the stick. Be sure to test all eight positions and that the Joystick centers when released. As the Trigger is pressed a red * will appear after the words FIRE-BUTTON. Failure of any of these actions indicates a faulty Joystick.

KEYBOARD TEST

This test is a verification test of all keyboard switches and special function switches; i.e., OPTION. This is the same test as the Self Test in OS resident. All keys and switches may be verified **except** BREAK and SYSTEM RESET. These are verified by correct operation. SYSTEM RESET should cause the system to reboot and return to Title Screen. BREAK will, as the prompt at the bottom of the screen states, return you to the INDIVIDUAL TESTS menu.

NOTE: The keyboard shown on the screen and in Figure 2-22 is for an ATARI 1200XL ™ Computer. Therefore, some keys shown will not function. As each key is pressed, the displayed key will flash to inverse video and a tone is heard. Remember, CONTROL and the SHIFT keys require an additional key be pressed AT THE SAME TIME. Failure of a key display and tone indicates the following possible failures:

1) Faulty keyboard key
2) Faulty keyboard cable
3) Faulty keyboard decoders
4) Faulty POKEY IC

Figure 2-22 shows the Keyboard Test Screen.

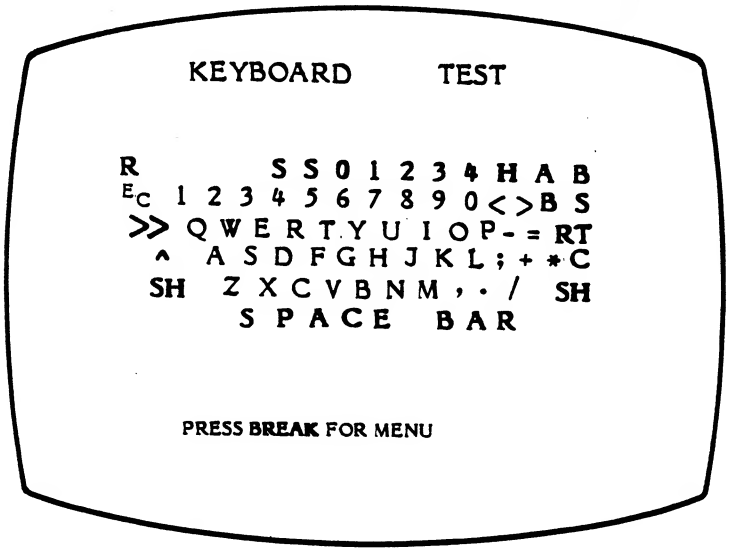


Figure 2-22. Keyboard Test Screen

MAINTENANCE MODE

There is no screen display or if you prefer, a solid black screen. Press any key (except BREAK or SYSTEM RESET) and a tone is heard. Press any key again. The tone stops.

This mode of operation allows the technician to measure the CH.2 and 4.5MHz carrier frequencies and adjust if necessary.

NOTE: Most state-of-the-art televisions require exact settings of these frequencies since they incorporate synthesized circuits. It is suggested that a frequency meter be used to measure these frequencies.

CH.2 = 61.25 MHz
Sound Carrier = 4.5MHz

Must use CH.2 due to modulator design.

Once alignment is complete, press any key to produce the tone. This is a verification test of proper alignment. If necessary, adjust television fine tuning to produce clear picture on channel 2.

PADDLE TEST

Figure 2-23 shows the Paddle Test Screen.

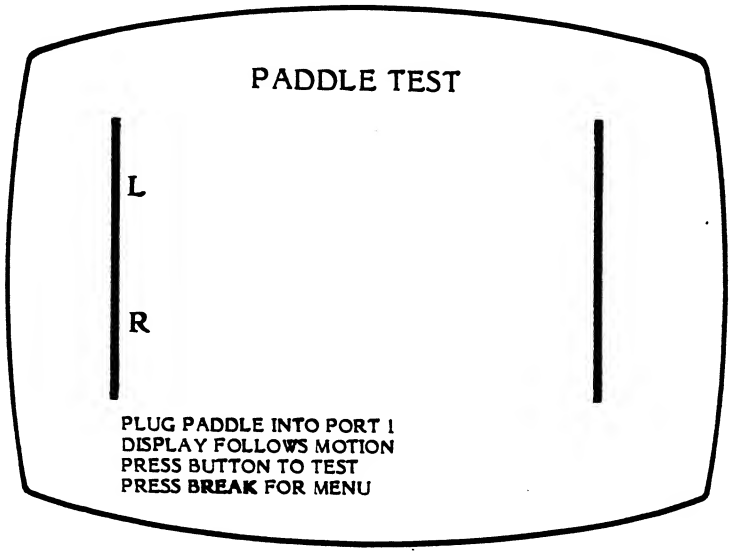


Figure 2-23. Paddle Test Screen

NOTE: This test assumes that the unit is working properly.

Insert the Paddle Controller plug into Port 1 on the console. The displayed characters, L & R, will follow the respective paddle movement as you turn the knob. The Trigger will cause the respective action. Any failure of these actions indicates a faulty Paddle Controller.

This completes the descriptions of all tests that may be performed on the unit. Additional testing is suggested using the EXTENDED UNIT TEST in conjunction with the CHANGE TEST OPTS menu for control. For example, the EXTENDED UNIT TEST should be used in CONTINOUS mode for burn-in testing. Be sure to define test execution, on the CHANGE TEST OPTS menu, to use or not use the Test Assembly as is appropriate.

CHANGE TEST OPTS & EXTENDED UNIT TEST

Figure 2-24 shows the Change Test Opts Screen.

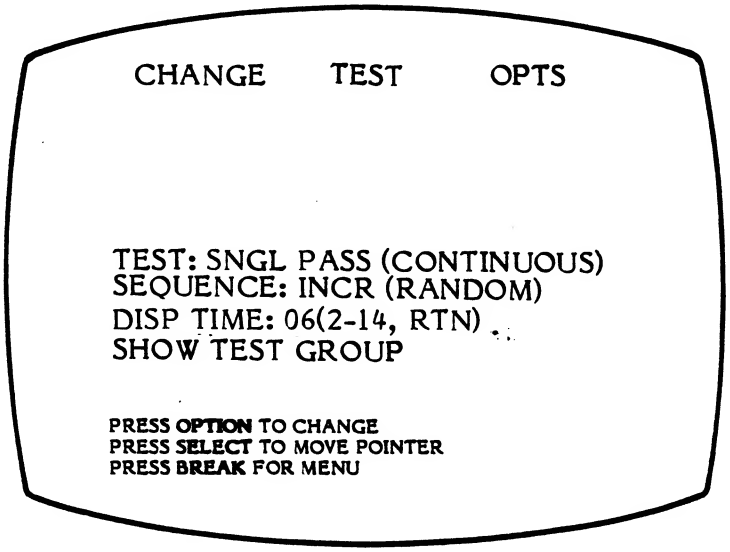


Figure 2-24. Change Test Opts Screen

At the bottom of the screen are instructions for changing test conditions or options.

Press the OPTION key to select SINGLE PASS or CONTINUOUS testing. Press the SELECT to move the pointer to SEQUENCE. Press OPTION to select either INCR, as defined by test group, or RANDOM which is a random selection of test within the limits of the test group used. Press SELECT to move the pointer to DISP TIME (display time). Press OPTION to select display time in seconds or indefinite. Time values are 2, 4, 6, 8, 10, 12, 14 seconds and RTN (RETURN key) for indefinite. Very Important: RTN option should not be used with any testing except INDIVIDUAL TESTS as it halts testing until the RETURN key is pressed.

Press SELECT to move the pointer to SHOW TEST GROUP. Press OPTION to display the menu (See Figure 2-25).

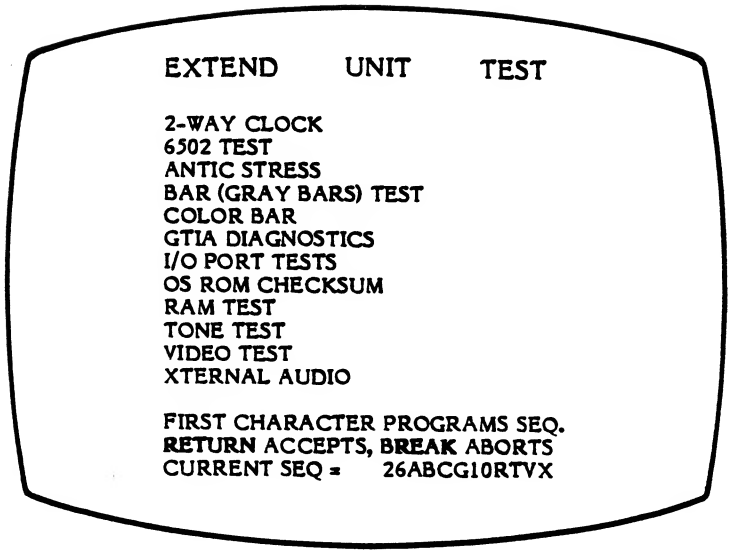


Figure 2-25. Extended Unit Test Screen (Selection)

The bottom of the screen shows the options. The first character of each test selects that test. The RETURN key ends entry of choices and causes diagnostics to use only those tests during EXTEND UNIT TEST. Use the DELETE key to erase choices listed at the bottom of the screen just behind the cursor. **Note:** If 2-WAY CLOCK TEST (2) and 6502 TEST (6) are not desired, DELETE must be used to erase all choices. Then each character except 2 and 6 (ABCGIORTVX) must be pressed followed by a RETURN. Press the BREAK key and return to the EXECUTIVE MENU. Press SELECT to move pointer to the EXTENDED UNIT TEST. Press OPTION to display the EXTENDED UNIT TEST menu shown in Figure 2-26.

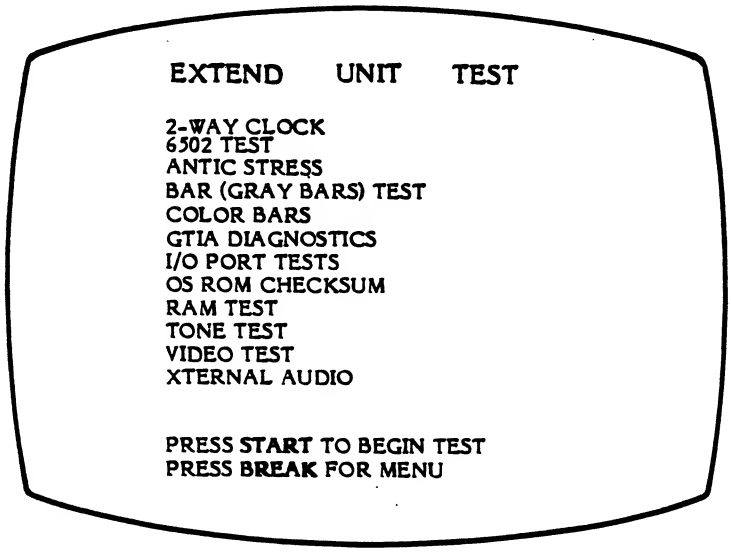


Figure 2-26. Extended Unit Test Screen

Since the CHANGE TEST OPTS menu has been used to select the particular test to be executed, this menu is not altered. However, testing proceeds according to test options definition. This test along with TEST OPTS may be used to execute one or any choices or combination of choices. It may be used to execute a test or tests, continuously to check for a particular intermittent failure or for burn-in.

SHOW ERR SUMMARY

Press BREAK to return to the EXECUTIVE MENU. Press SELECT to move the pointer to the SHOW ERR SUMMARY. Press OPTION to begin display of error summaries shown in Figures 2-27 thru 2-35.

NOTE: I/O voltage error display is shown only on I/O Port Tests Screen (Voltage Test), Figure 2-12.

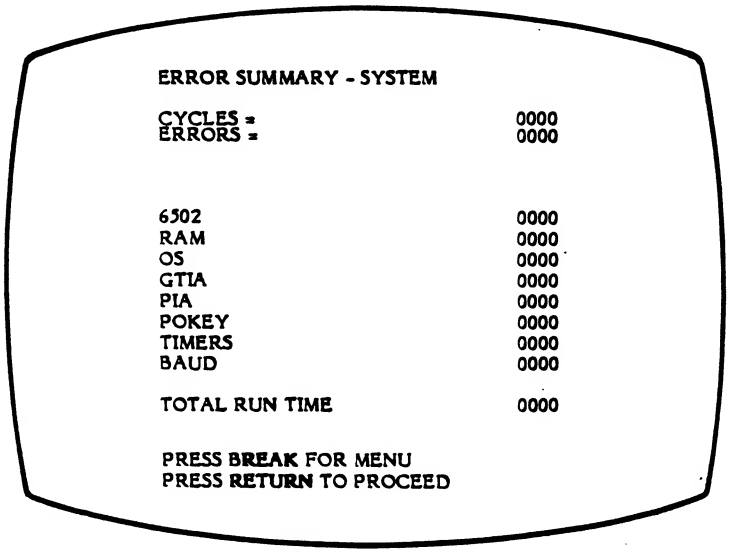


Figure 2-27. System Error Summary Screen

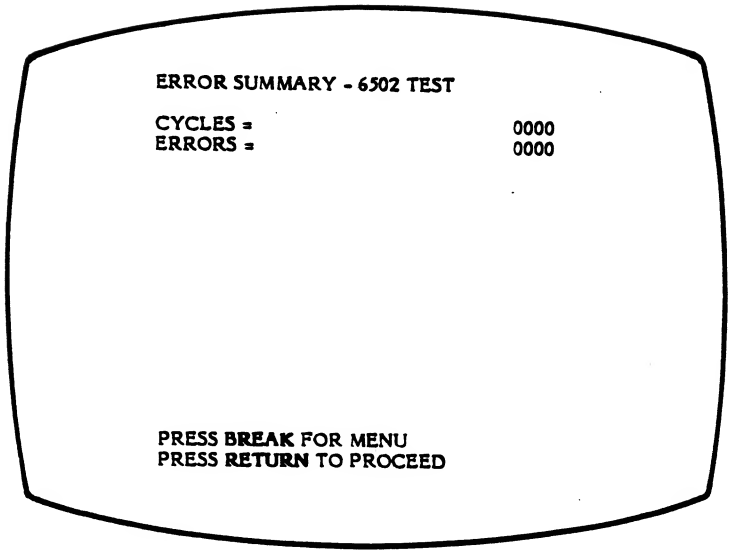


Figure 2-28. 6502 Error Summary Screen

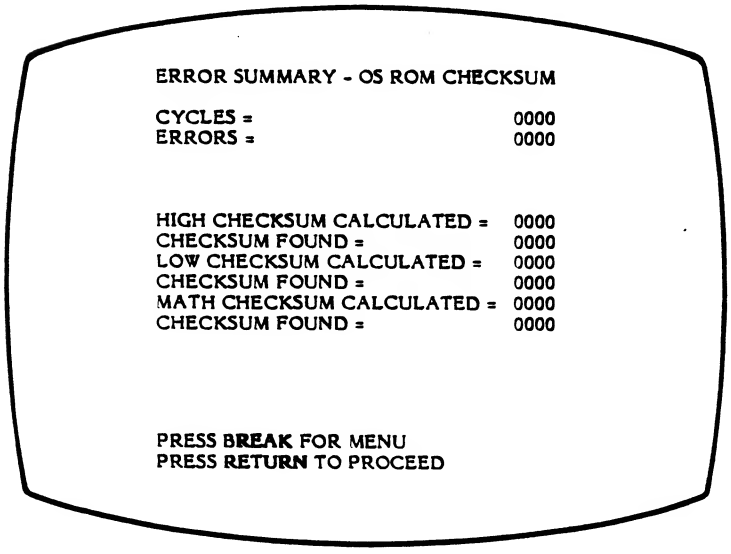


Figure 2-29. OS ROM Checksum Error Summary Screen

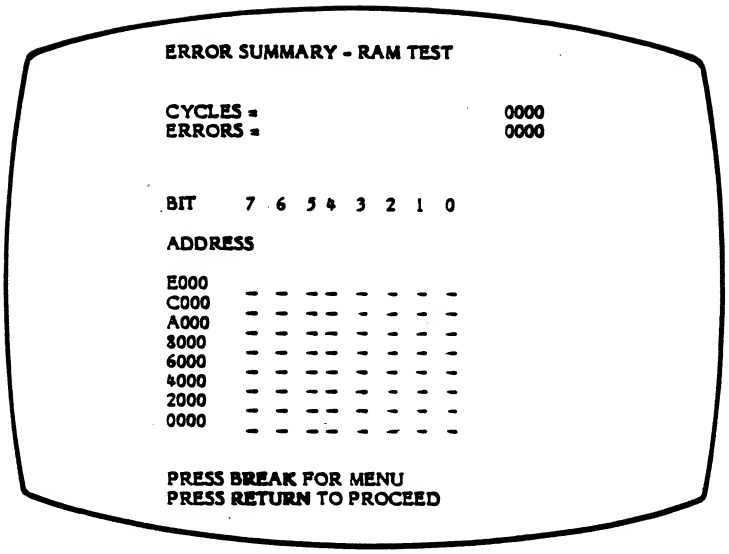


Figure 2-30. RAM Error Summary Screen

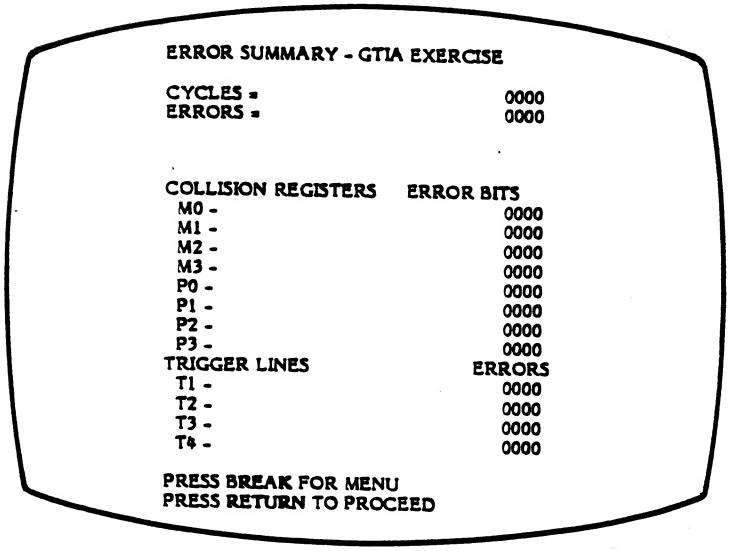


Figure 2-31. GTIA Error Summary Screen

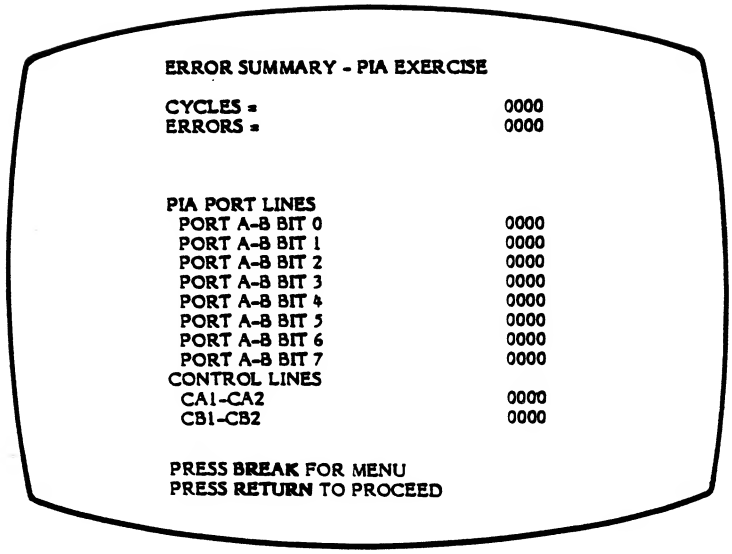


Figure 2-32. PIA Error Summary Screen

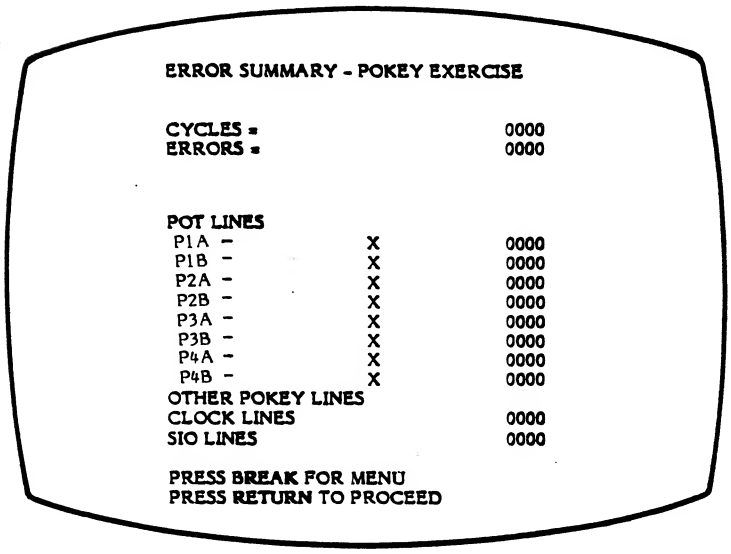


Figure 2-33. POKEY Error Summary Screen

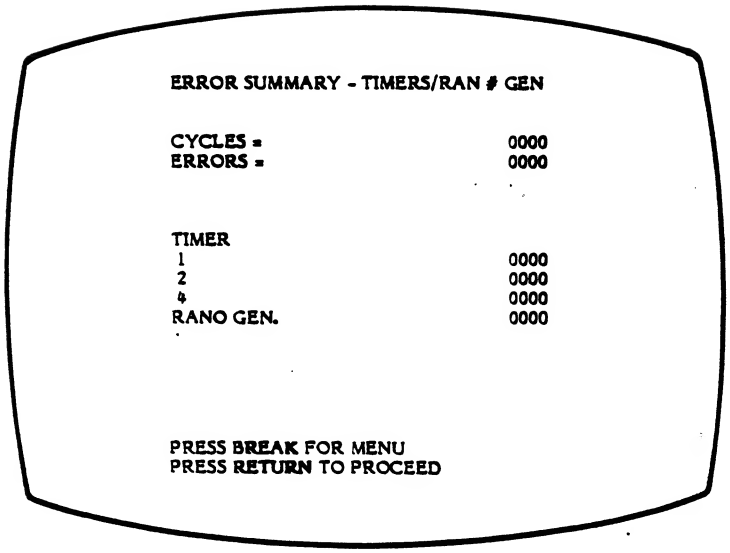


Figure 2-34. Timers/RAN # Gen Error Summary Screen

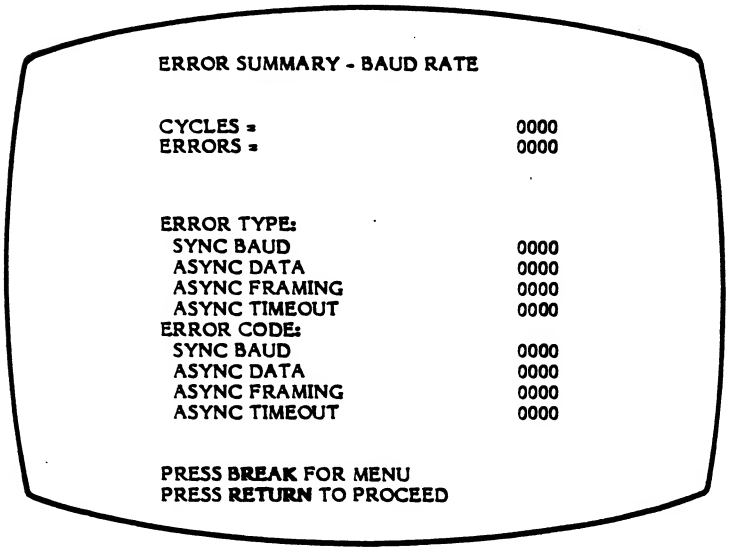


Figure 2-35. Baud Rate Error Summary Screen

POT LINE failures shown in Figure 2-34 decode as follows:

A = Possible short to +5V
B = Time constant too long
D = Time constant too short
E = A & D

These Error Summaries are useful in pin-pointing the exact cause of failure. Most tests have sub-tests whose failures are listed in the error summary.

Important: All error summary tables are zeroed when SYSTEM RESET is used and during power-up. Do not use SYSTEM RESET to return to EXECUTIVE MENU if accurate error reporting is desired.

FATAL SYSTEM ERROR DEFINITIONS

(What the system was trying to do when it happened)

CODE	FUNCTIONAL TEST IN PROGRESS
04	Refresh Check on Pattern "FF"
05	Address Line Check (could not get "unique" addresses using each line)
06	Address Line Check (could not get "unique" addresses using each line)
07	Data Line Check (one or more stuck hi or lo)
08	Refresh test in pattern "00"
09	RAM somewhere in page 0 or 1
10	RAM failure in page 0 (approx area $004D $007F)
11	RAM failure in page 0 (approx area $004D $007F)
17	RAM failure in page 0 (address $0038) Data read = data stored
18	Ram failure in page 0 (address $0019) Data read = data stored
97*	Not enough stack entries present (same as 98, in different terms)
98*	Stack overflow or underflow has occurred.
99*	RAM error in page 1 or system has taken a bad branch somewhere.

*97, 98, 99 related to address decoding on ROM or RAM or to bad CPU

This concludes the instructions for using SuperSALT and the SuperSALT Test Assembly.

For further assistance call:

Inside California
(800) 672-1466

Outside California
(800) 538-1535

SECTION 3

SUPERSALT TEST ASSEMBLY INSPECTION, AND CALIBRATION PROCEDURE

INSPECTION PROCEDURE

1) Remove the Test Assembly PCBA from static foam

2) Inspect component side of the PCBA for:

   a) Proper component orientation
      - o diodes polarized properly
      - o electrolytic capacitors polarized properly
      - o components down against PC Board
      - o all switches & jacks mounted correctly

   b) Reject any incorrect PCBA - NOTE the problem

3) Inspect solder side of the PCBA for:

   a) cold solder joints

   b) solder splashes

   c) solder bridges

   d) excessive solder flux residue

   e) Reject any incorrect PCBAs - NOTE the problem

CALIBRATION PROCEDURE

Use 800 Console Only - Known Good

1) Connect the AC power adaptor into either J7 or J8, and the AC jumper into the other of the two jacks.

2) Connect the other end of the AC jumper cable into the CPU and turn on the power.

3) Connect the DC power source to J6 (Test Assembly) and turn on SW1. This powers up the CPS SuperSALT Test Assembly.

4) Set volt meter to a scale greater than 10 volts DC.

5) Connect volt meter GND lead to GND on the Test Assembly PC Board (the neg side of C17).

6) Connect volt meter positive lead to TP1 and adjust R41 for a 6.00 VDC reading.

7) Connect volt meter positive lead to TP2 and adjust R52 for a 2.5 VDC reading using an ATARI 800 w/48K. No cartridge should be installed in the CPU.

8) Connect the volt meter positive lead to TP3 and adjust R53 for a 2.5 VDC reading. Repeat step 7 & 8 until balanced.

SECTION 4

DRAWINGS

The schematic is attached to the front cover of this manual. Remove it and place it in this section.

SECTION 5

SERVICE BULLETINS

This section is to be used by you to file the three classifications of service bulletins that are periodically released by the Director of Technical Support.

The following are brief descriptions of each classification:

FIELD CHANGE ORDER

A Field Change Order describes mandatory hardware or software changes to ATARI products and instructs how to implement these changes. The changes must be performed on all units serviced or repaired.

UPGRADE BULLETIN

An Upgrade Bulletin describes product improvements or modifications that the consumer may wish to purchase. These bulletins allow you to modify the customer's unit to add capabilities which may not have been available when the unit was originally manufactured.

TECH TIP

A Tech Tip is a document of a general nature which transmits routine service or repair information. By communicating methods developed since you attended training classes, Tech Tips aid to continuously improve repair skills and increase knowledge of ATARI products.

Other times, Tech Tips alert you to units that have been modified and are now standard for ATARI Manufacturing, but are different from many existing units and require different repair techniques.

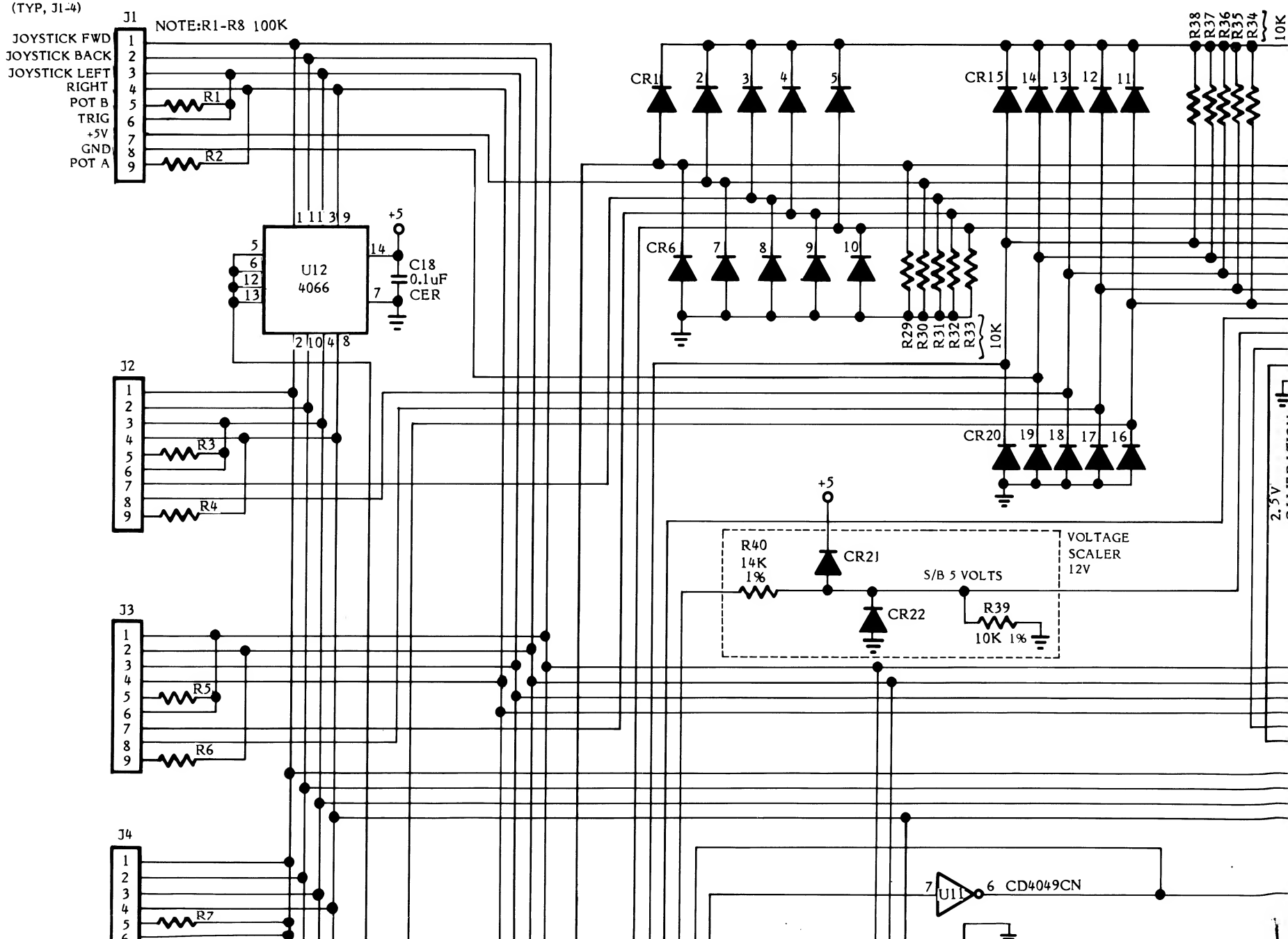
ATARI SUPERSALT MISC

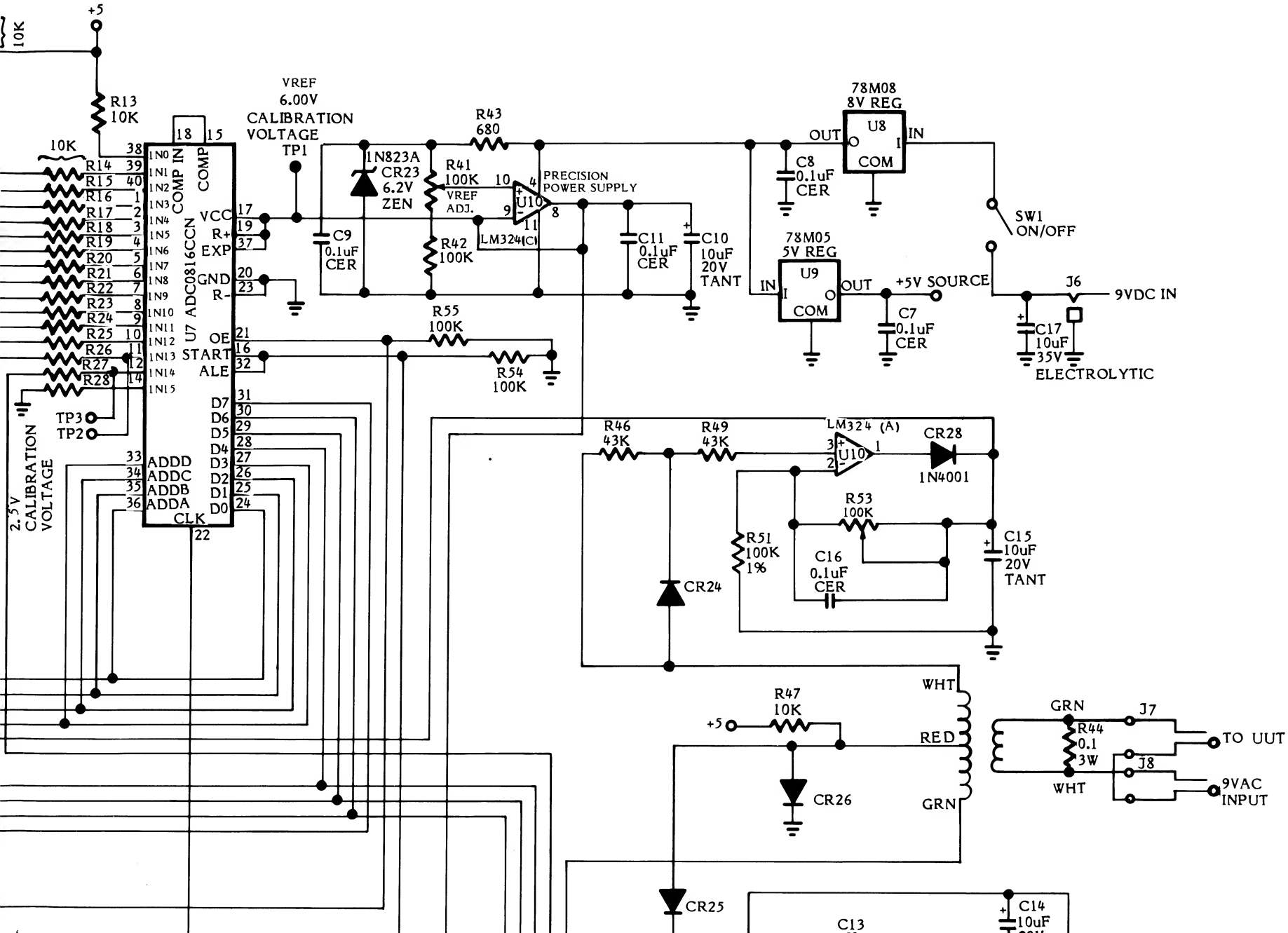
SUPERSALT CORRECTION FOR BAUD ERROR

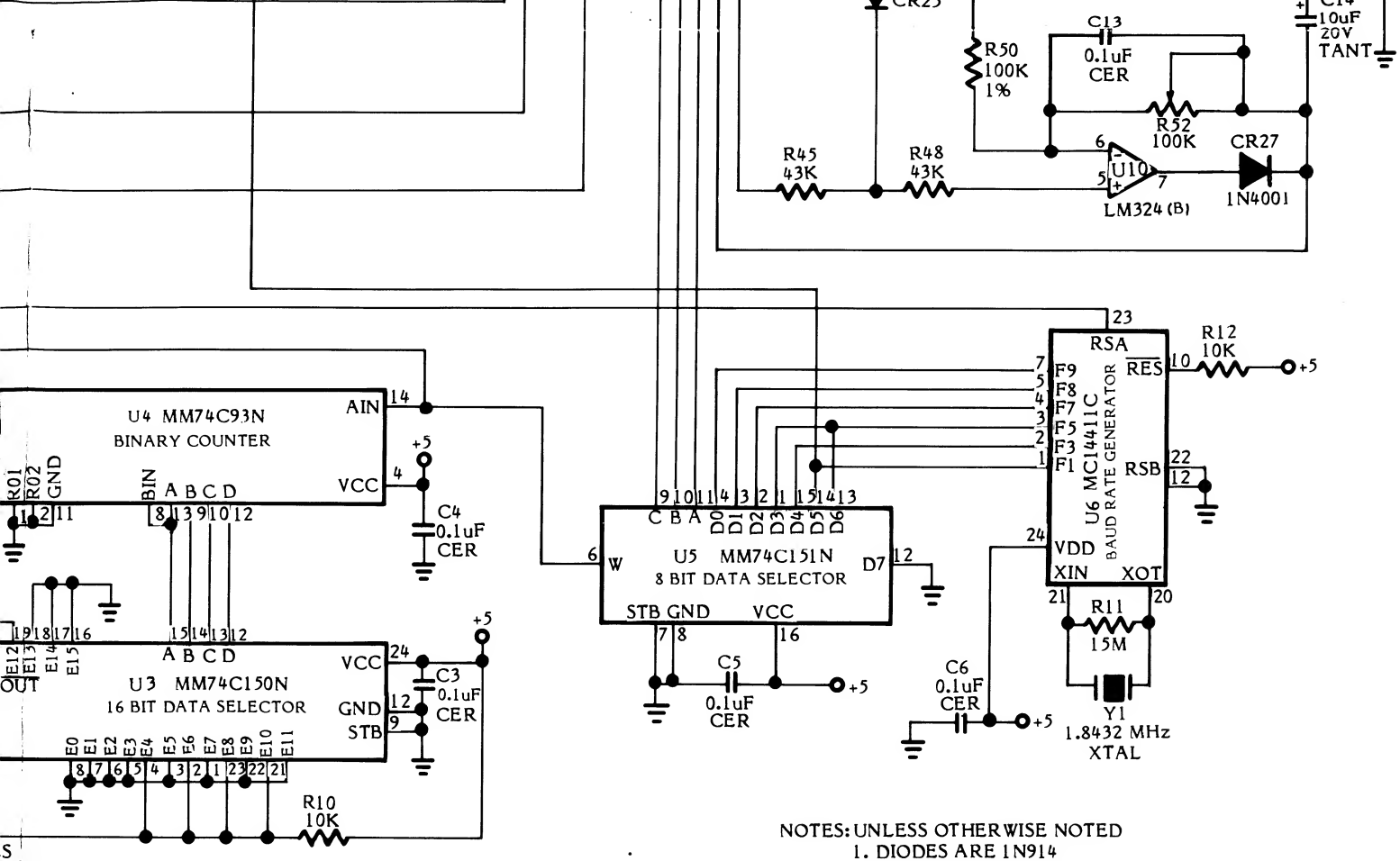
1. SOLDER JUMPER WIRE FROM PIN 2 TO PIN 4 ON U3

ATARI SUPERSALT TEST

SUPERSALT PERFORMANCE TEST WITH CARTRIDGE ONLY
1. ERRORS DISPLAYED- GTIA-4/PIA-8/POKEY-5/BAUD-2


(TYP, J1-4)
J1
NOTE:R1-R8 100K
JOYSTICK FWD
JOYSTICK BACK
JOYSTICK LEFT
RIGHT
POT B
TRIG
+5V
GND
POT A
R1
R2
U12
4066
C18
0.1uF
CER
J2
R3
R4
J3
R5
R6
J4
R7
CR1
CR15
CR6
CR20
R29
R30
R31
R32
R33
10K
R34
R35
R36
R37
R38
10K
R40
14K
1%
CR21
S/B 5 VOLTS
CR22
R39
10K 1%
VOLTAGE
SCALER
12V
2.5V
U11
CD4049CN

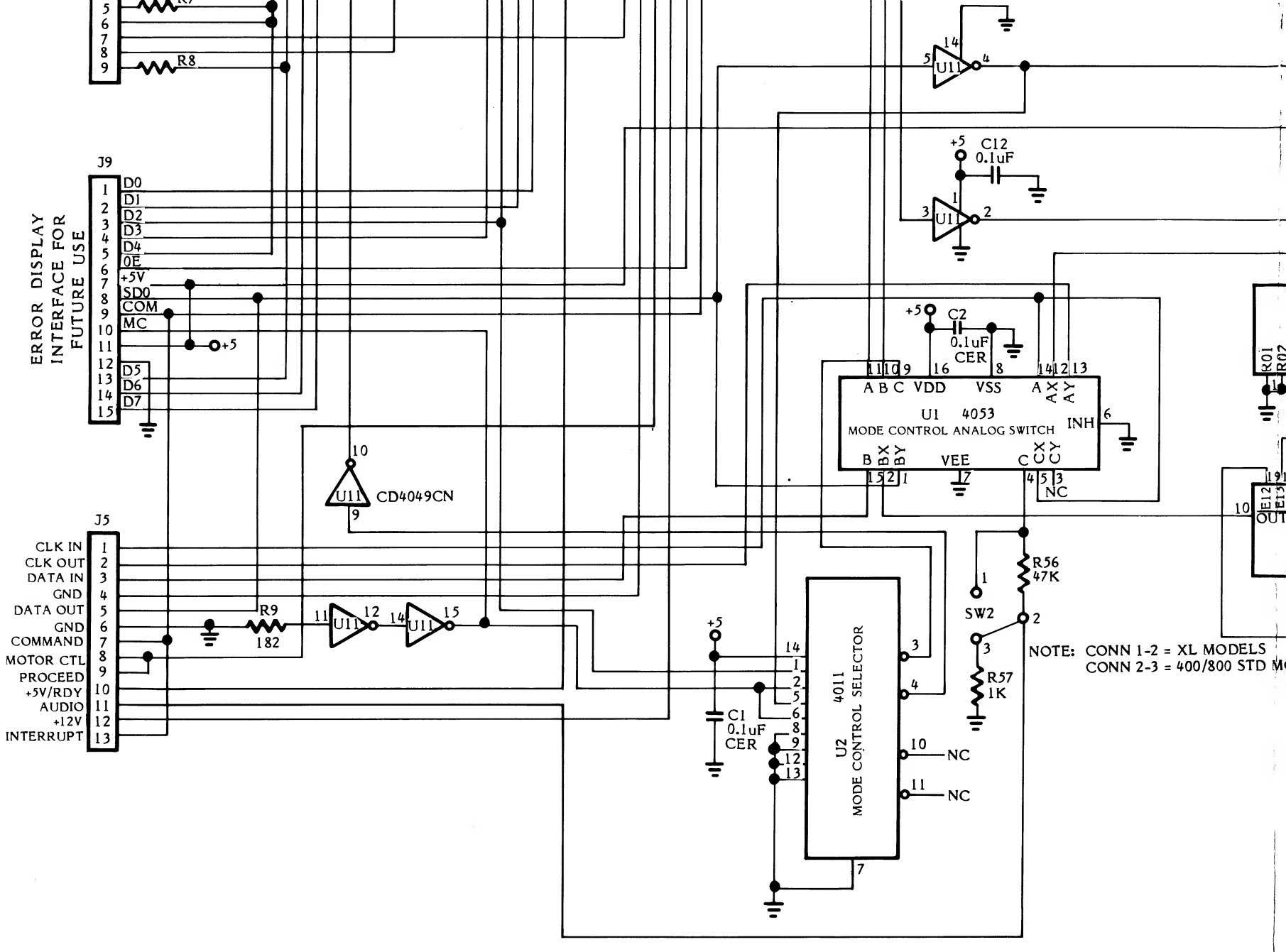

+5
10K
R13
10K
10K
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
TP3
TP2
2.5V
CALIBRATION
VOLTAGE
U7 ADC0816CCN
COMP IN
COMP
VCC
R+
EXP
GND
R-
OE
START
ALE
D7
D6
D5
D4
D3
D2
D1
D0
CLK
ADDD
ADDC
ADDB
ADDA
VREF
6.00V
CALIBRATION
VOLTAGE
TP1
1N823A
CR23
6.2V
ZEN
R43
680
R41
100K
VREF
ADJ.
R42
100K
U10
LM324(C)
PRECISION
POWER SUPPLY
C9
0.1uF
CER
C11
0.1uF
CER
C10
10uF
20V
TANT
78M08
8V REG
U8
OUT
IN
COM
C8
0.1uF
CER
SW1
ON/OFF
78M05
5V REG
U9
IN
OUT
COM
+5V SOURCE
C7
0.1uF
CER
J6
9VDC IN
C17
10uF
35V
ELECTROLYTIC
R55
100K
R54
100K
R46
43K
R49
43K
LM324 (A)
U10
CR28
1N4001
R53
100K
R51
100K
1%
C16
0.1uF
CER
C15
10uF
20V
TANT
CR24
R47
10K
+5
WHT
RED
GRN
CR26
GRN
J7
R44
0.1
3W
J8
WHT
TO UUT
9VAC
INPUT
CR25
C13
C14
10uF



NOTES: UNLESS OTHERWISE NOTED
1. DIODES ARE 1N914
2. RESISTOR VALUES ARE IN OHMS 1/4 W 5%

S
D MODELS

CPS SUPERSALT PCBA


ERROR DISPLAY INTERFACE FOR FUTURE USE
J9
D0
D1
D2
D3
D4
0E
+5V
SD0
COM
MC
D5
D6
D7
R8
+5
J5
CLK IN
CLK OUT
DATA IN
GND
DATA OUT
GND
COMMAND
MOTOR CTL
PROCEED
+5V/RDY
AUDIO
+12V
INTERRUPT
R9
182
U11
CD4049CN
C12
0.1uF
C2
0.1uF
CER
U1 4053
MODE CONTROL ANALOG SWITCH
A B C VDD VSS A AX AY
B BX BY VEE C CX CY
INH
NC
U2 4011
MODE CONTROL SELECTOR
C1
0.1uF
CER
SW2
R56
47K
R57
1K
NC
NOTE: CONN 1-2 = XL MODELS
CONN 2-3 = 400/800 STD M